

[AX216B-SP-100]



AX216B U-Disk Controller Product Specification

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AX216B U-Disk Controller

CPU Features

- 8-bit 8051 CPU, with enhance extend instruction, optimized for USB, NAND Flash applications
- All instructions are single-cycled except branching instructions
- MAX 96 MIPS performance with on chip PLL

General I/O

- 32 GPIO pins
- All GPIO pins can be programmable as input or output individually
- All GPIO pins are internal pull-up selectable individually
- CMOS / TTL level input

USB Interface Features

- Built-in USB controller and USBPHY
- Fully supports USB2.0 device
- Support 4 Endpoint (EP 0/1/2/3), every Endpoint support both TX and RX transaction

NAND Flash Interface Features

- Supports 528/2K/4K/8K bytes page NAND flash
- Supports SLC, MLC, TLC NAND flash
- Supports Two-Plane or Interleave NAND flash
- Supports X8/X16 NAND flash
- Supports parallel mode
- Supports up to 8 CE
- Built-in 31bit/page(1K bytes) on-the-fly ECC
- Data protection during data transfer if unplugged/power off

Low Power Consumption

- Operating frequency variable 12-96MHz
- Supports Sleep Mode and Idle mode
- Fast wake up during Sleep Mode

Other Features

- Supports 1 timer
- Built-in 12MHz OSC
- Built-in UART
- Built-in PLL
- Built-in LED driver
- Built-in POR and BOR
- Built-in 3.3V to 1.8V LDO

Package

- Die form
- LQFP 48 pin

Temperature

- Operating temp.: 0°C to +70°C
- Storage temp.: -40°C to +125°C

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1 Product Overview

1.1 Description

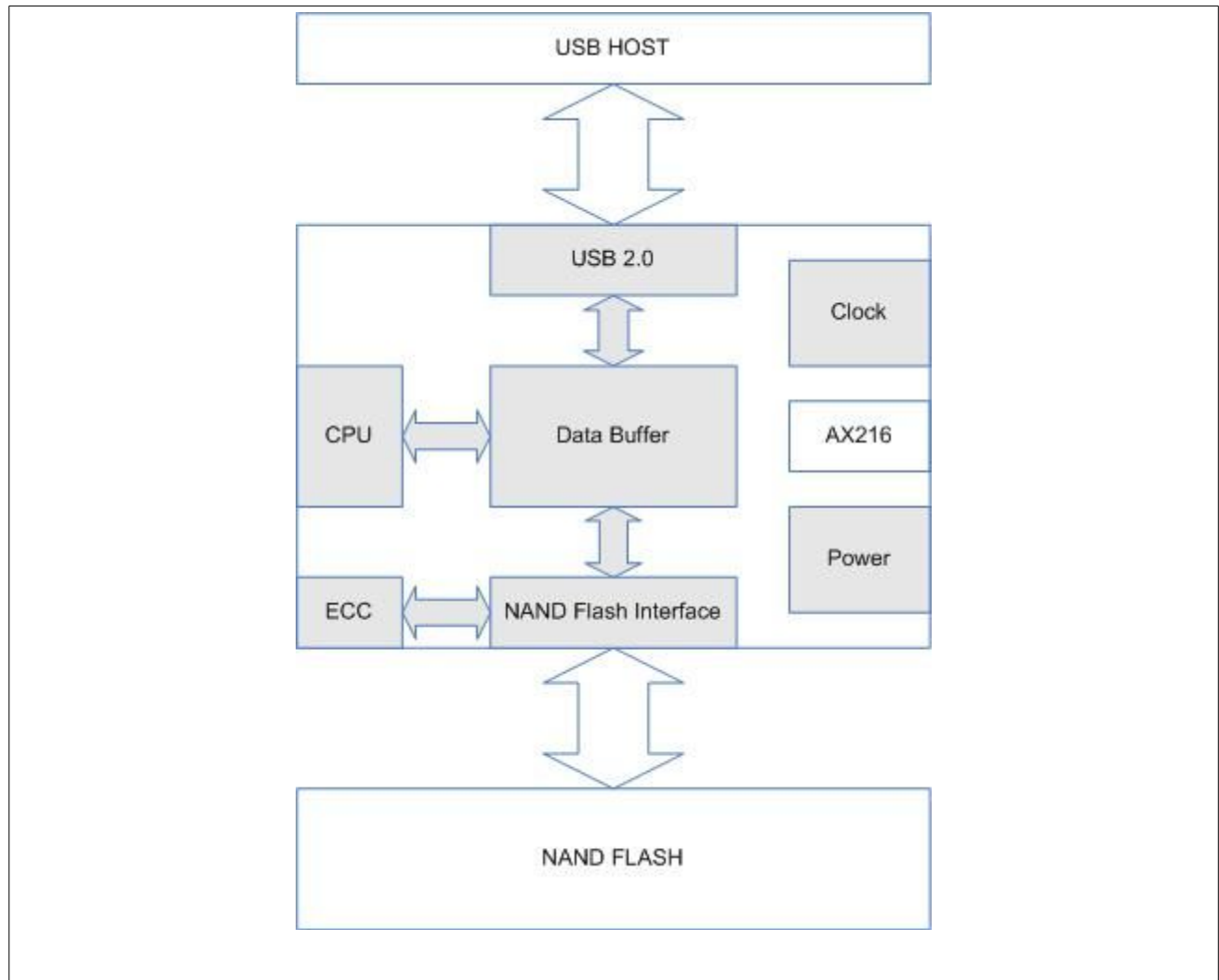
AX216B is a 8-bit 8051 microcontroller. It integrates advanced digital and analog peripherals to accommodate USB applications.

Features:

- 8-bit 8051 CPU, with enhance extend instruction, optimized for USB, NAND flash control
- All instructions are single-cycled except branching instructions
- Fully supports USB2.0 device
- Supports high capacity standard
- Enhanced ESD protection
- Supports 528/2K/4K/8K bytes page NAND Flash
- Supports SLC/MLC/TLC NAND flash
- Supports X8/X16 flash data bus
- Supports up to 8 flash chips
- Supports SPI flash
- Supports 17/25/29/31 bits on-the-fly ECC per sector
- Data protection during data transfer even if unplugged/power off
- Built-in OSC
- Built-in PLL
- Built-in POR and BOR
- Built-in Regulator
- Built-in 3.3V Power Gate
- Supports Idle mode and Sleep mode
- Supports iNAND, Ex3 flash

1.2 System Architecture

Figure 1-1: System Block Diagram



2 Pin Information

2.1 Pin Assignment

2.1.1 TQFP48

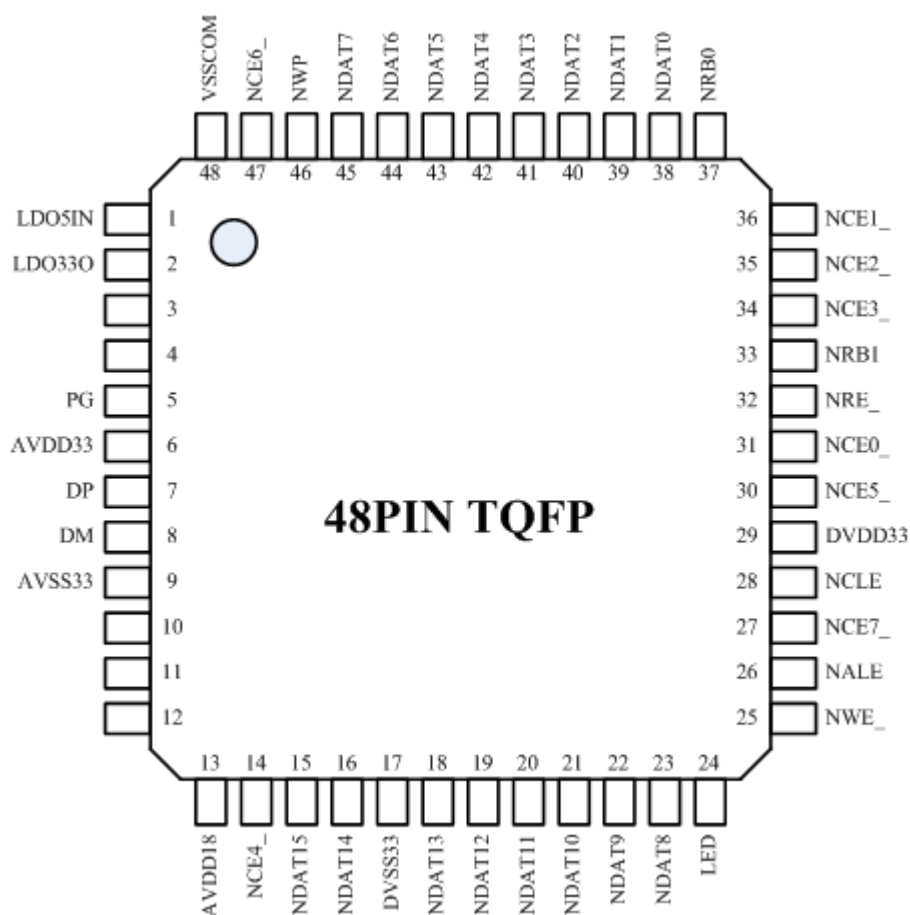


Figure 2-1: TQFP 48 Pin Assignment

2.2 Pin Description

Table 2-2: 48Pin Description

Pin	Symbol	Direction	Description
1	LDO5IN	PWR	Regulator 5V Power input
2	LDO33O	PWR	Regulator 3.3V Power output

3	NC	--	--
4	NC	--	--
5	PG	PWR	3.3V Power gate output
6	AVDD33	PWR	3.3V Power
7	DP	I/O	USB Data D+
8	DM	I/O	USB Data D-
9	AVSS33	GND	Analog Ground
10	NC	--	--
11	NC	--	--
12	NC	--	--
13	VDD18	PWR	1.8V power
14	NCE4_	I/O	NAND Flash chip enable – chip 4 SPI DI1 GPIO port04
15	NDAT15	I/O	NAND Flash data bus bit 15 PHY ANALOG TEST PIN GPIO port27
16	NDAT14	I/O	NAND Flash data bus bit 14 system clock output GPIO port26
17	DVSS33	GND	Digital 3.3V Ground
18	NDAT13	I/O	NAND Flash data bus bit 13 PIN mode select GPIO port25
19	NDAT12	I/O	NAND Flash data bus bit 12 GPIO port24
20	NDAT11	I/O	NAND Flash data bus bit 11 GPIO port23
21	NDAT10	I/O	NAND Flash data bus bit 10 GPIO port22
22	NDAT9	I/O	NAND Flash data bus bit 9 GPIO port21
23	NDAT8	I/O	NAND Flash data bus bit 8 GPIO port20
24	LED	I/O	LED output UART TX SPI DO1 GPIO port37
25	NWE_	I/O	NAND Flash write enable GPIO port33
26	NALE	I/O	NAND Flash address latch enable SPI DO GPIO port32

27	NCE7_	I/O	NAND Flash chip enable – chip 7 GPIO port07
28	NCLE	I/O	NAND Flash command latch enable GPIO port31
29	DVDD33	PWR	Digital 3.3V Power
30	NCE5_	I/O	NAND Flash chip enable – chip 5 SPI CLK1 GPIO port05
31	NCE0_	I/O	NAND Flash chip enable – chip 0 GPIO port00
32	NRE_	I/O	NAND Flash read enable SPI CLK GPIO port34
33	NRB1	I/O	NAND Flash ready_busy 1 GPIO port36
34	NCE3_	I/O	NAND Flash chip enable – chip 3 GPIO port03
35	NCE2_	I/O	NAND Flash chip enable – chip 2 GPIO port02
36	NCE1_	I/O	NAND Flash chip enable – chip 1 GPIO port01
37	NRB0	I/O	NAND Flash ready_busy 0 SPI DI GPIO port35
38	NDAT0	I/O	NAND Flash data bus bit 0 GPIO port10
39	NDAT1	I/O	NAND Flash data bus bit 1 GPIO port11
40	NDAT2	I/O	NAND Flash data bus bit 2 GPIO port12
41	NDAT3	I/O	NAND Flash data bus bit 3 GPIO port13
42	NDAT4	I/O	NAND Flash data bus bit 4 GPIO port14
43	NDAT5	I/O	NAND Flash data bus bit 5 GPIO port15
44	NDAT6	I/O	NAND Flash data bus bit 6 GPIO port16
45	NDAT7	I/O	NAND Flash data bus bit 7 GPIO port17
46	NWP	I/O	NAND Flash write protect GPIO port30
47	NCE6_	I/O	NAND Flash chip enable – chip 6 GPIO port37

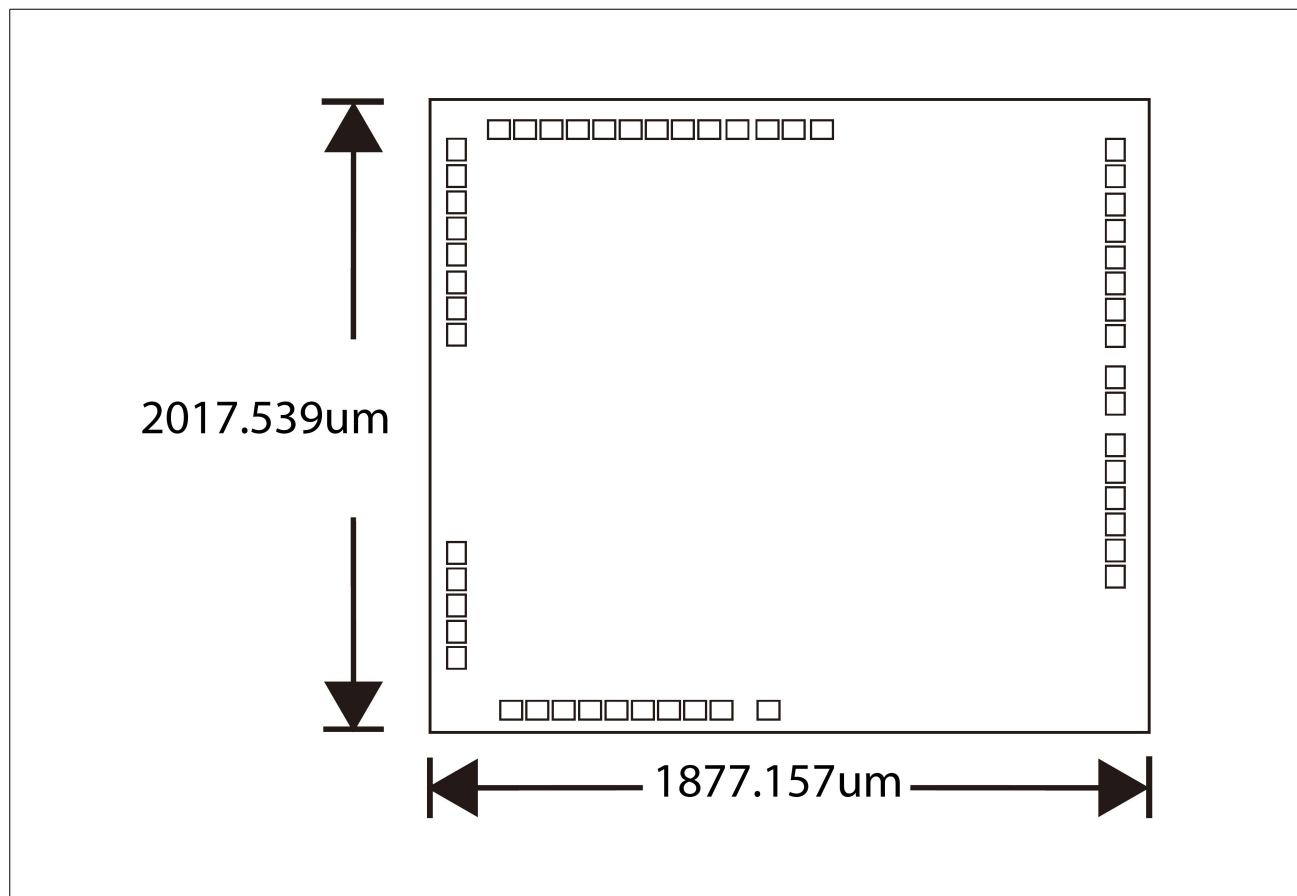
48	VSSCOM	GND	Common Ground
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Table 2-4: Port Mapping

Function 1	Function 2	Function 3	Function 4
P0.0	NCE0		
P0.1	NCE1		
P0.2	NCE2		
P0.3	NCE3		
P0.4	NCE4		SPIDI1
P0.5	NCE5		SPICLK1
P0.6	NCE6		SDCLK
P0.7	NCE7		SDCMD
P1.0	NDAT0		
P1.1	NDAT1		
P1.2	NDAT2		
P1.3	NDAT3		
P1.4	NDAT4		
P1.5	NDAT5		
P1.6	NDAT6		
P1.7	NDAT7		
P2.0	NDAT8		SDDAT0
P2.1	NDAT9		SDDAT1
P2.2	NDAT10		SDDAT2
P2.3	NDAT11		SDDAT3
P2.4	NDAT12		
P2.5	NDAT13	PIN mode select	
P2.6	NDAT14	system clock output	
P2.7	NDAT15	VATEST	
P3.0	NWP		
P3.1	NCLE		
P3.2	NALE	SPI DO	
P3.3	NWE		
P3.4	NRE	SPI CLK	
P3.5	NRB0	SPI DI	
P3.6	NRB1		
P3.7	LED	UTX	SPIDO1

2.3 Die Schematic

Figure 2-1: AX216 Die Schematics



2.4 PAD Coordinate

Table 2-1: PAD Coordinate

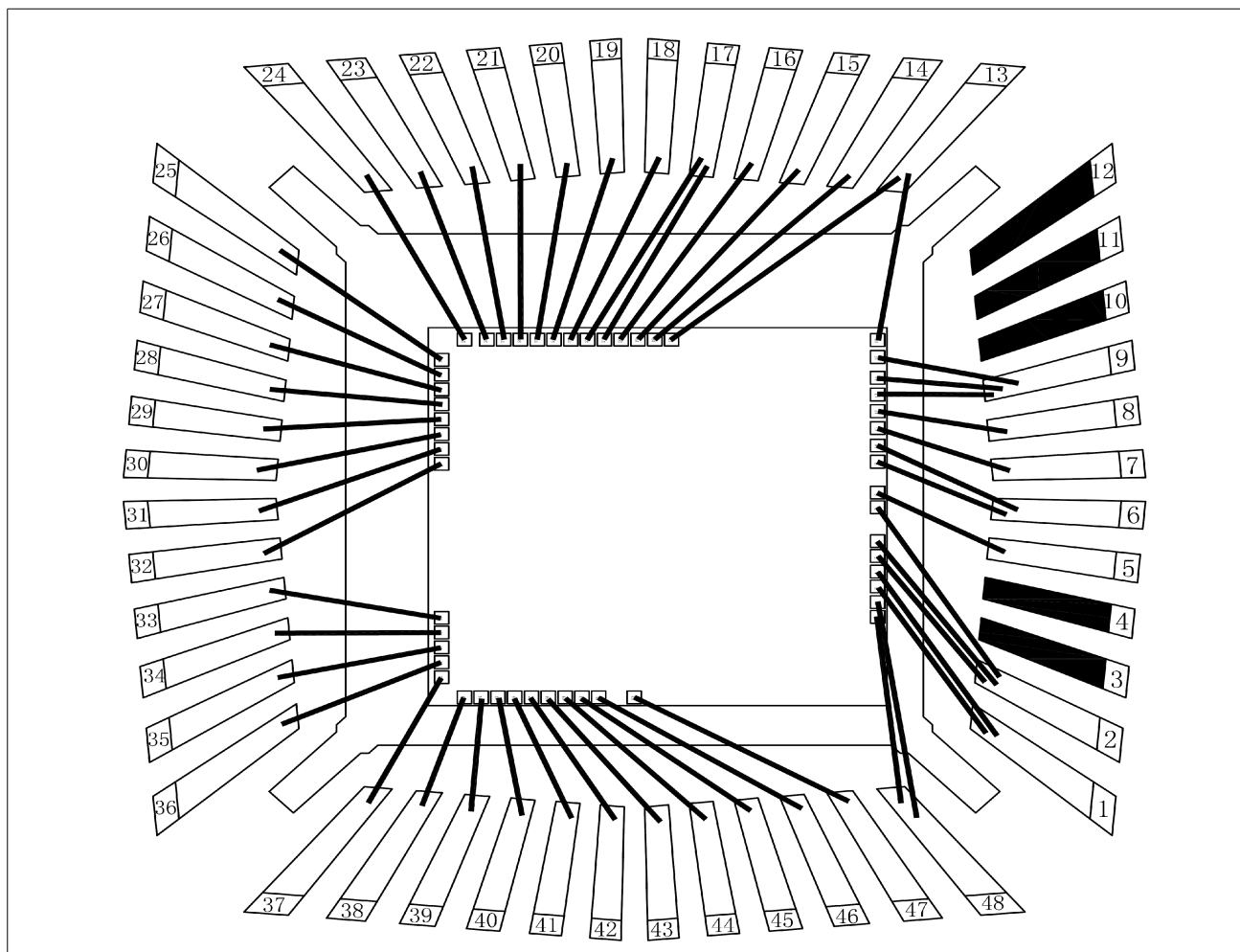
	X (um)	Y (um)
VSSIO	440.1225	40.977
VSS	513.9405	40.977
VDDLDO	591.7365	40.977
VDDLDO	665.5005	40.977
VDDIO	742.8825	40.977
VDDIO	816.714	40.977

VDDIO	985.1175	40.977
PG	1057.568	40.977
vdda33t	1210.779	40.977
vdda33c	1291.311	40.977
DP	1377.95	40.977
DM	1461.65	40.977
VSSA33T	1544.652	40.977
VSSA33C	1627.655	40.977
VS18	1730.628	40.977
VD18	1815.435	40.977
VDD	1817.406	947.0745
NCE4_	1817.406	1020.87
NDAT15	1817.406	1094.67
NDAT14	1817.406	1168.47
VSSIO	1817.406	1242.275
VSS	1817.406	1316.075
NDAT13	1817.406	1389.87
NDAT12	1817.406	1463.67
NDAT11	1817.406	1537.47
NDAT10	1817.406	1611.27
NDAT9	1817.406	1685.07
NDAT8	1817.406	1758.87
LED	1817.406	1857.861
NWE_	1717.488	1957.788

NALE	1643.688	1957.788
NCE7_	1569.888	1957.788
NCLE	1496.088	1957.788
VDDIO	1422.288	1957.788
NCE5_	1348.488	1957.788
NCE0_	1274.688	1957.788
NRE_	1200.888	1957.788
NRB1	436.05	1957.788
NCE3_	363.2445	1957.788
NCE2_	289.4445	1957.788
NCE1_	215.6445	1957.788
NRB0	140.85	1957.788
NDAT0	40.9365	1857.87
NDAT1	40.9365	1784.07
NDAT2	40.9365	1710.27
NDAT3	40.9365	1636.47
NDAT4	40.9365	1562.67
NDAT5	40.9365	1488.87
NDAT6	40.9365	1415.07
NDAT7	40.9365	1341.27
NWP_	40.9365	1267.47
NCE6_	40.9365	1110.681

2.5 Bonding Diagram

Figure 2-2: AX216B Bonding Diagram



3 Electrical Characteristics

3.1 Absolute Maximum Ratings

Symbol	Parameter	MIN	MAX	Unit
VDD	DC Power Supply	-0.3	+5.5	V
Vin	Input Voltage	VSS-0.3	VDD+0.3	V
Vout	Output Voltage	VSS-0.3	VDD+0.3	V
Ta	Operating Temperature	-25	+85	°C
Tst	Storage Temperature	-40	+125	°C

3.2 Recommended Operating Conditions

Symbol	Parameter	MIN	TYP	MAX	Unit
VDD50	Supply Voltage	4.0	5	5.5	V
VDD33	Supply Voltage	3.0	3.3	3.6	V
VDD18	Supply Voltage	1.62	1.8	1.98	V
Vin	Input Voltage	0	-	VDD	V
Tamb	Ambient Temperature	0	-	+70	°C

3.3 Electrical Characteristics of 3.3V I/O Cell

Symbol	Parameter	CONDITIONS	Limits			Unit
			MIN	TYP	MAX	
VDD	Power Supply	3.3V I/O	3.0	3.3	3.6	V
Vil	Input Low Voltage	LVTTL			0.8	V
Vih	Input High Voltage		2			V
Vol	Output Low Voltage	I _{ol} =2~16mA			0.4	V
Voh	Output High Voltage	I _{oh} =2~16mA	2.4			V
Rpu	Input Pull-up Resistance	Vin = 0		30K		ohm

Appendix I Revision History

Date	Version	Revised items	Revised by
16/12/2010	0.0.1	1.First draft	Rimsky Cheng

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