

# **USB 2.0 Flash Controller Specification**

## **UP14**

**Version 1.1**

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## **A. General Description**

The UP14 micro-controller supports USB 2.0 & 1.1 and interface to NAND Flash Memory. This chip is specially designed for portable storage device or build-in to the PC / Notebook / IA system.

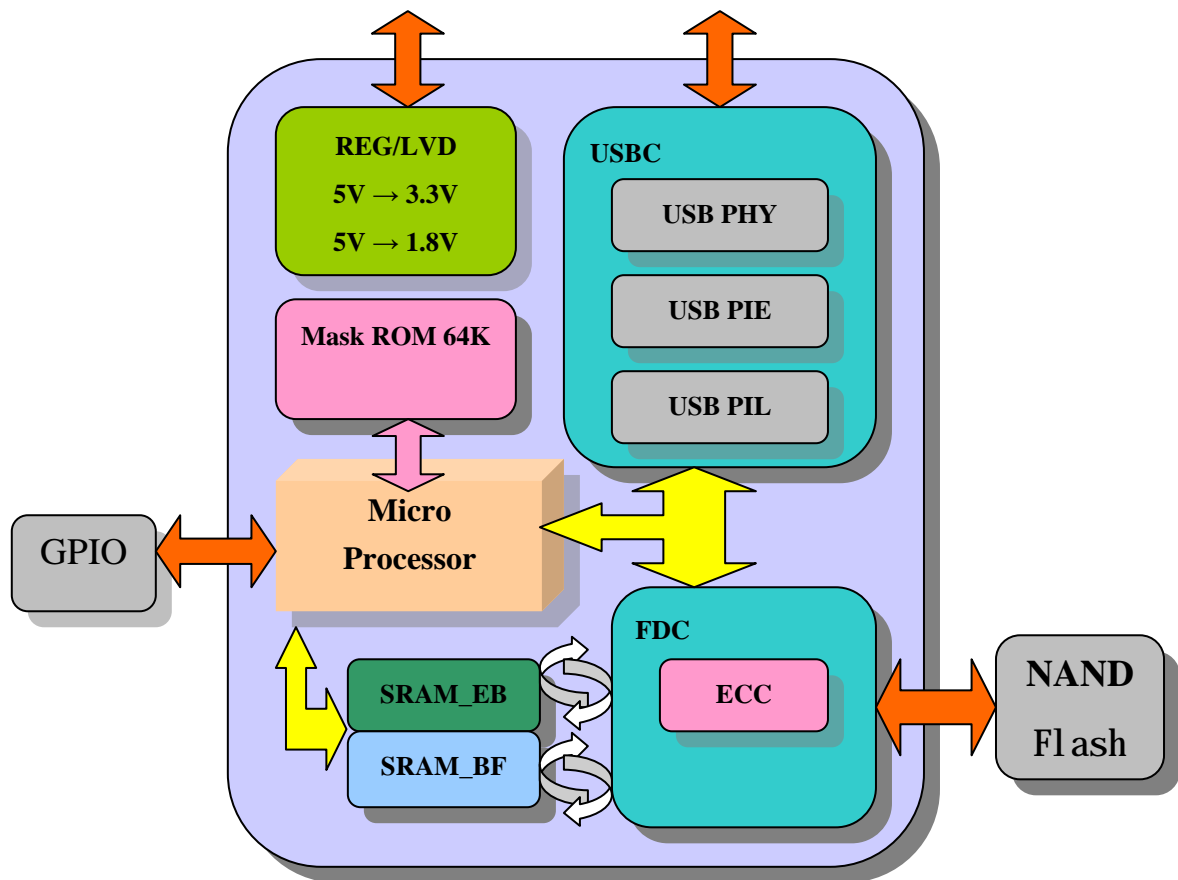
By using this single chip solution, it will reduce a lot of efforts which was needed from R/D to production, as well as simplifying the RMA problems. With the USB plug & play function and driver-less solution with most of the operating systems, this solution provides not only easy to install, but also fast, easy to use and low cost way for user.

## B. Controller Features

- 2 **Support Host Interfaces : USB 2.0 & 1.1 Interface**
- 2 **Support Flash Memory Interfaces : Build-in NAND Flash Memory**
  - Build-in hardware ECC circuit (BCH 3/6/12 bit).
  - Support all types of Flash SLC Small/Large Block NAND Flash.
  - Support MLC Small/ Large Block NAND flash.
  - Dual channels are available for all package types.
  - Support Programmable Flash r/w timing & EDO read timing.
- 2 **USB Interface :**
  - Fully compatible with USB Specification Version 2.0 & 1.1
  - Complies with high speed USB 2.0 with build-in high/full speed transceiver & SIE
  - High speed 480Mbit/second supporting
  - Full speed 12Mbit/second supporting
  - Support one CONTROL transfer, one INTERRUPT transfer and two BULK transfer
  - Support four Endpoints :
    - ü Endpoint 0 : 64 Bytes CONTROL transfer
    - ü Endpoint 1 : 512 Bytes BULK transfer for IN transaction
    - ü Endpoint 2 : 512 Bytes BULK transfer for OUT transaction
    - ü Endpoint 3 : 64 Bytes INTERRUPT transfer for IN transaction
  - Support USB power saving mode
- 2 **Build-In NAND Flash Memory Interface**
  - Build-in hardware ECC circuit.
  - Support SLC (Single level cell) 2k-page large block NAND Flash.
  - Support SLC (Single level cell) 4k-page large block NAND Flash.
  - Support MLC (Multi level cell) 2k-page Large Block NAND flash.
  - Support MLC (Multi level cell) 4k-page Large Block NAND flash.

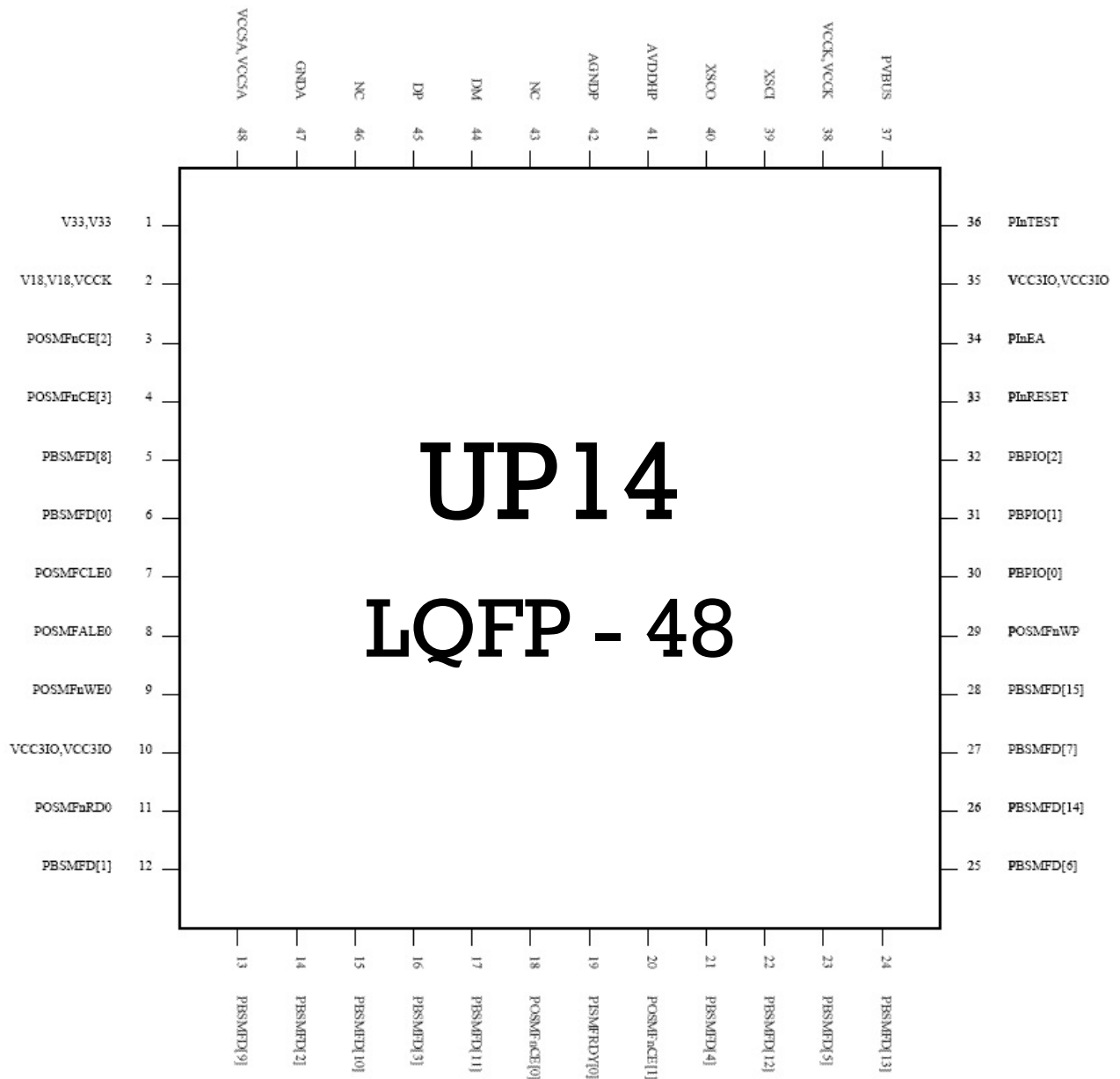
- ² **Mask ROM : 64KB Mask ROM** for control f/w.
- ² **Buffer SRAM : 8 buffers** for performance improvement
- ² **On Chip Regulator : Cost effective solution**
- ² **Support 3.3V Flash I/O:**  
Internal 3.3V regulator can supply current for controller analog circuit, controller I/O and Flash.
- ² **Support 1.8V Flash I/O:**  
Internal 1.8V regulator can supply the current for controller core, controller I/O and Flash.
- ² **48-pins QFP Package**
- ² **Operating Voltage: 4.5~5.5V.**
- ² **USB bus-powered capability.**
- ² **Power Saving implemented.**
- ² **Working Frequency: 12MHz.**

## C. BLOCK DIAGRAM



## D. Pin Assignment and Description

### D1. Pin Assignment - 48pins



**D2. Pins Listed in Numeric Order – 48pins**

<b>Pin</b>	<b>Signal</b>	<b>Pin</b>	<b>Signal</b>	<b>Pin</b>	<b>Signal</b>
1	V33	17	PBSMFD[11]	33	PIInRESET
2	V18/VCKK	18	POSMFnCE[0]	34	PIInEA
3	POSMFnCE[2]	19	PISMFRDY[0]	35	VCC3IO
4	POSMFnCE[3]	20	POSMFnCE[1]	36	PIInTEST
5	PBSMFD[8]	21	PBSMFD[4]	37	PVBUS
6	PBSMFD[0]	22	PBSMFD[12]	38	VCKK
7	POSMFCLE0	23	PBSMFD[5]	39	XSCI
8	POSMFALE0	24	PBSMFD[13]	40	XSCO
9	POSMFnWE0	25	PBSMFD[6]	41	VCC33A_HSRT
10	VCC3IO	26	PBSMFD[14]	42	GND33A_HSRT
11	POSMFnRD0	27	PBSMFD[7]	43	NC
12	PBSMFD[1]	28	PBSMFD[15]	44	DM
13	PBSMFD[9]	29	POSMFnWP	45	DP
14	PBSMFD[2]	30	PBPIO[0]	46	NC
15	PBSMFD[10]	31	PBPIO[1]	47	GND33A_PLL/GNDA
16	PBSMFD[3]	32	PBPIO[2]	48	VCC5A



### D3. Pin Description

USB + Regulator Interface		
Pin Name	Dir.	Pin Description
V18	VCC18	1.8V regulator power supply
V33	VCC33	3.3V regulator power supply
VCC5A	VCC5	5.0V regulator power input
GND A	GND	0V regulator ground reference input
DP	I/O	USB 2.0 data in positive pin terminal.
DM	I/O	USB 2.0 data in negative pin terminal.
RREF	I	Connect to external reference resistor(12K±1%) to GND.
VCC33A_HSRT	VCC33	USB 2.0 IO power (3.3V)
GND33A_HSRT	GND	USB 2.0 IO ground reference (0V)
VCC33A_PLL	VCC33	USB 2.0 PLL power (3.3V)
GND33A_PLL	VCC33	USB 2.0 PLL ground (0V)
XSCO	O	Crystal oscillator output
XSCI	I	Crystal oscillator input
VCCK	I	USB 2.0 core power (1.8V)
NC		No Connection

FLASH Interface		
Pin Name	Dir.	Pin Description
POSMFnCE[3:0]	O	Flash chip enable, low active.
PBSMFD[15:0]	I/O	Flash data bus
POSMFALE0, POSMFALE1	O	Flash address latch enable, high active.
POSMFCLE0, POSMFCLE1	O	Flash command latch enable, high active.
POSMFnRD0, POSMFnRD1	O	Flash read control signal, low active.
POSMFnWE0, POSMFnWE1	O	Flash write control signal, low active.
POSMFnWP	O	Flash write protect control signal, low active.
PISMFRDY[0]	I	Flash ready/busy signal input

Global Signal		
Pin Name	Dir.	Pin Description
PInRESET	I	Reset Signal
PInTEST	I	Test Mode Signal.
PInEA	I	EAMODE Select Signal.
PVBUS	I	USB VBUS input
PBPIO[7:0]	I/O	8-bit GPIO
VCC3IO	VCC33	3.3V IO power
VCCK	VCC18	1.8V digital core power
VSSIO	GND	0V IO ground reference
VSSK	GND	0V digital core ground reference

## E. System Power Consumption

Item	Power Consumption (mA)	
	1 * Flash	2 * Flash
Normal	66.00	67.03
Suspend	0.38	0.39
Sleep	0.38	0.38
Read	91.08	104.12
Write	93.88	118.74
Un-configured	42.24	42.46

The above values are for reference only, it may change according to the flash memory used.

## F. Electrical Specifications

### Absolute Maximum Rating

Item	Symbol	Parameter	MIN	MAX	Unit
1	$V_{DD}-V_{SS}$	DC Power Supply	-0.3	+5.5	V
2	$V_{IN}$	Input Voltage	$V_{SS}-0.3$	$V_{DD}+0.3$	V
3	$T_a$	Operating Temperature (Commercial)	0	+70	°C
4	$T_a$	Operating Temperature (Industrial)	-40	+85	°C
5	$T_{st}$	Storage Temperature (Commercial)	-40	+85	°C
6	$T_{st}$	Storage Temperature (Industrial)	-50	+125	°C

Parameter	Symbol	Min	Typ	MAX	Unit
Operating Temperature (Commercial)	$T_a$	0	+25	+70	°C
Operating Temperature (Industrial)	$T_a$	-40	+25	+85	°C
$V_{DD}$ Voltage	$V_{DD}$	3.0	3.3	3.6	V
		4.5	5.0	5.5	V

## G. DC Characters

### DC characteristics of 3.3V I/O Cells

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
V <sub>CK</sub>	Core Power Supply	Core Area	1.62	1.8	1.98	V
V <sub>CC3IO</sub>	Power Supply	3.3V I/O	3.0	3.3	3.6	V
Temp	Junction Temperature		0	25	115	°C
V <sub>t</sub>	Switching threshold	LVTTL		1.5		V
V <sub>t-</sub>	Schmitt Trigger Negative Going threshold voltage	LVTTL	0.8	1.1		V
V <sub>t+</sub>	Schmitt Trigger Positive Going threshold voltage			1.6	2.0	V
V <sub>ol</sub>	Output Low voltage	I <sub>ol</sub>   = 2 ~ 16 mA			0.4	V
V <sub>oh</sub>	Output High voltage	I <sub>oh</sub>   = 2 ~ 16 mA	2.4			V
R <sub>pu</sub>	Input Pull-Up Resistance	PU=high, PD=low	40	75	190	KΩ
R <sub>pd</sub>	Input Pull-Down Resistance	PU=high, PD=low	40	75	190	KΩ
I <sub>in</sub>	Input Leakage Current	V <sub>in</sub> = V <sub>CC3I</sub> or 0			1	μA
I <sub>oz</sub>	Tri-state Output Leakage Current		-10	±1	10	μA

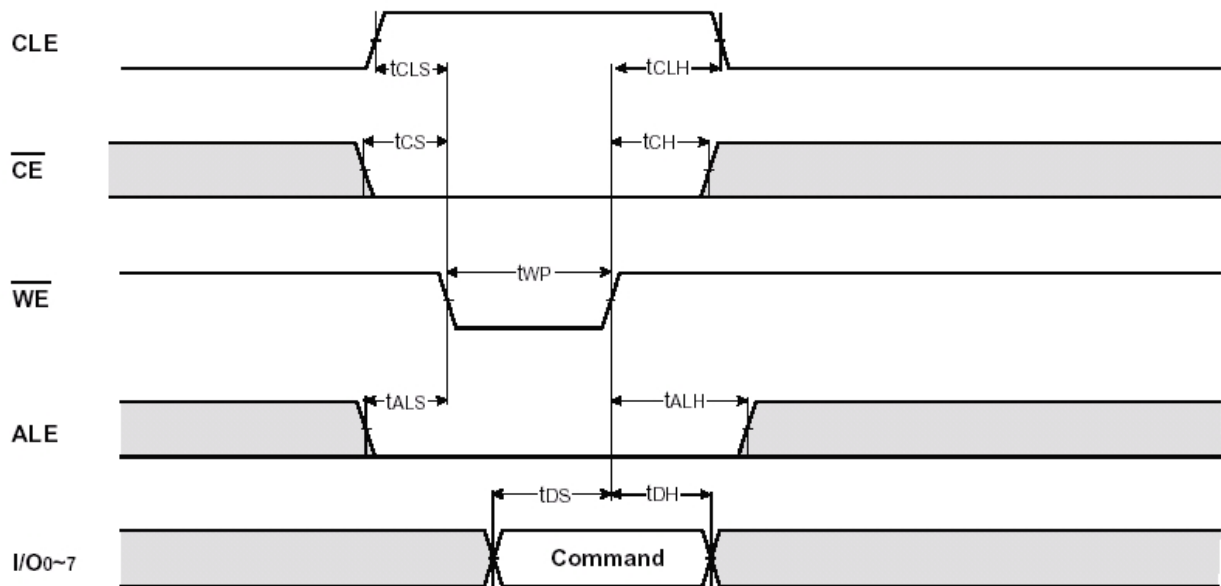
## H. AC Characters

### H1. Flash Memory Interface Timing

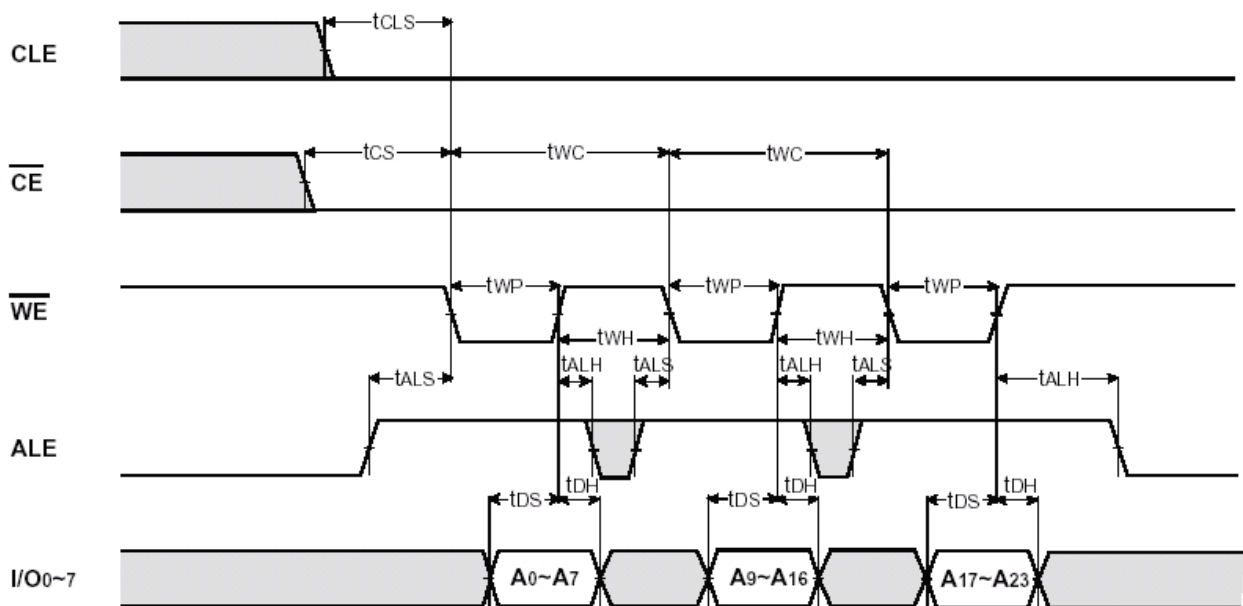
#### *NAND Flash Memory Interface Timing*

Parameter	Symbol	Min	Max	Unit
CLE Set-up Time	$t_{CLS}$	12	-	ns
CLE Hold Time	$t_{CLH}$	12	-	ns
CE Setup Time	$t_{CS}$	20	-	ns
CE Hold Time	$t_{CH}$	12	-	ns
WE Pulse Width	$t_{WP}$	12	-	ns
ALE Setup Time	$t_{ALS}$	12	-	ns
ALE Hold Time	$t_{ALH}$	12	-	ns
Data Setup Time	$t_{DS}$	12	-	ns
Data Hold Time	$t_{DH}$	10	-	ns
Write Cycle Time	$t_{WC}$	25	-	ns
WE High Hold Time	$t_{WH}$	10	-	ns
Read Cycle Time	$t_{RC}$	25	-	ns
/RE Pulse Width	$t_{RP}$	12	-	ns
/RE High Hold Time	$t_{REH}$	10	-	ns
Ready to /RE Low	$t_{RR}$	50	-	ns

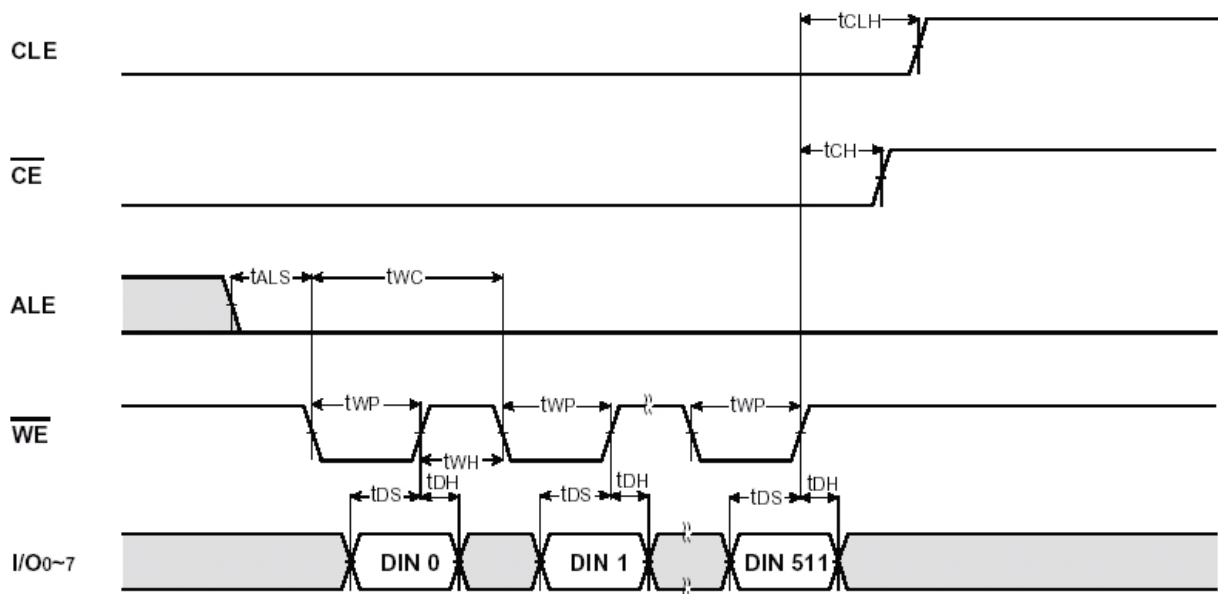
## H1.1 Command Latch Cycle



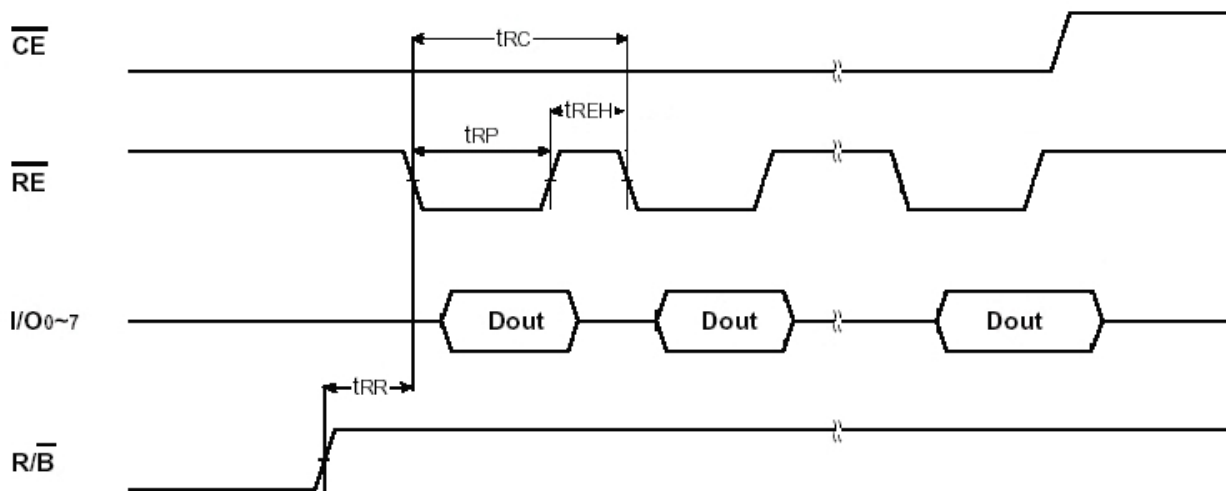
## H1.2 Address Latch Cycle



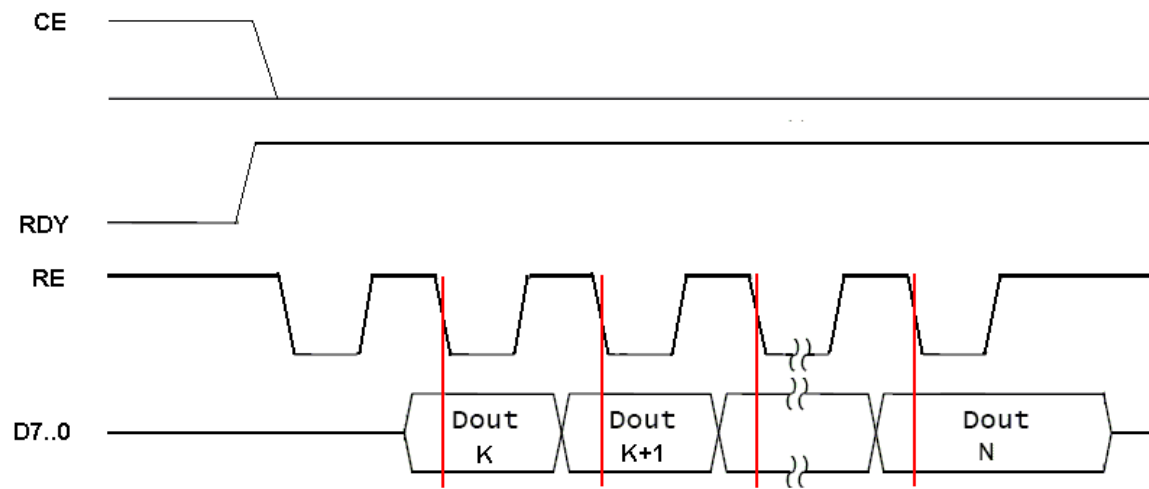
### H1.3 Input Data Latch Cycle



### H1.4 Sequential Out Cycle after Read (CLE=L, $\overline{\text{WE}}$ =H, ALE=L)



### H1.5 EDO mode for data latch



EDO mode to latch the data at the negative edge of RE.

# I. Package Information

## 11. 48 Pins

