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## **Phison Electronics Corporation**

# **USB 2.0 Flash Controller Specification PS2231**

**Version 1.6**

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**Document Number : S-07074**

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## **Revision History**

<b>Revision</b>	<b>History</b>	<b>Draft Date</b>	<b>Author</b>
1.0	First Release	21-Dec-06	Hughman
1.1	Add U3 Related Functions	27-Mar-07	Hughman
1.2	Add 48pin Controller Information	12-Jun-07	David
1.3	Modify Package Information	27-Jun-07	David
1.4	Modify Power Consumption	05-Jul-07	David
1.5	Modify Pin Description	31-Aug-07	Alex
1.6	Modify Electrical Specification	22-Oct-07	David

## **A. General Description**

The PHISON's PS2231 micro-controller supports USB 2.0 & 1.1 and interface to NAND Flash Memory. This chip is specially designed for portable storage device or build-in to the PC / Notebook / IA system. It is pin compatible to PS2134 & PS2135 & PS2136.

By using this single chip solution, it will reduce a lot of efforts which was needed from R/D to production, as well as simplifying the RMA problems. With the USB plug & play function and driver-less solution with most of the operating systems, this solution provides not only easy to install, but also fast, easy to use and low cost way for user.

## B. Controller Features

- ² **Support Host Interfaces :** USB 2.0 & 1.1 Interface
- ² **Support USB HID transport:** endpoint 3
- ² **Compliant to U3 Spec:**
  - 1024-bit RSA hardware module
  - 256-bit AES hardware module
  - Hidden area secure page
  - Password with AES encryption in private area
  - CD writing and CD lock/unlock
  - Trusted host ID for open private area
  - Random number hardware module
- ² **Support Flash Memory Interfaces :** Build-in NAND Flash Memory
- ² **USB Interface :**
  - Fully compatible with USB Specification Version 2.0 & 1.1
  - High speed 480Mbit/second supporting
  - Full speed 12Mbit/second supporting
  - Support one CONTROL transfer, one INTERRUPT transfer and two BULK transfer
  - Support four Endpoints :
    - λ Endpoint 0 : 64 Bytes CONTROL transfer
    - λ Endpoint 1 : 512 Bytes BULK transfer for IN transaction
    - λ Endpoint 2 : 512 Bytes BULK transfer for OUT transaction
    - λ Endpoint 3 : 64 Bytes INTERRUPT transfer for IN transaction
  - Support Data Payload
    - λ Endpoint 0 : max 64 bytes
    - λ Endpoint 1 : max 512 bytes
    - λ Endpoint 2 : max 512 bytes
    - λ Endpoint 3 : max 64 bytes
  - Support USB power saving mode

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## **2 Build-In NAND Flash Memory Interface**

- Build-in hardware ECC circuit.
- Support SLC (Single level cell) 2k-page large block NAND Flash.
- Support SLC (Single level cell) 4k-page large block NAND Flash.
- Support MLC (Multi level cell) 2k-page Large Block NAND flash.
- Support MLC (Multi level cell) 4k-page Large Block NAND flash.

## **2 Support In-System Programming through USB Port**

### **2 Transfer Rate for USB Interface:**

- “High speed” Up to 480Mbps/sec for USB 2.0
- “Full speed” Up to 12Mbps/sec for USB 1.1

### **2 Support 3.3V Flash I/O:**

Internal 3.3V regulator can supply current for controller analog circuit, controller I/O and Flash.

### **2 Support 1.8V Flash I/O:**

Internal 1.8V regulator can supply the current for controller core, controller I/O and Flash.

## **2 48-pins / 64-pins QFP Package**

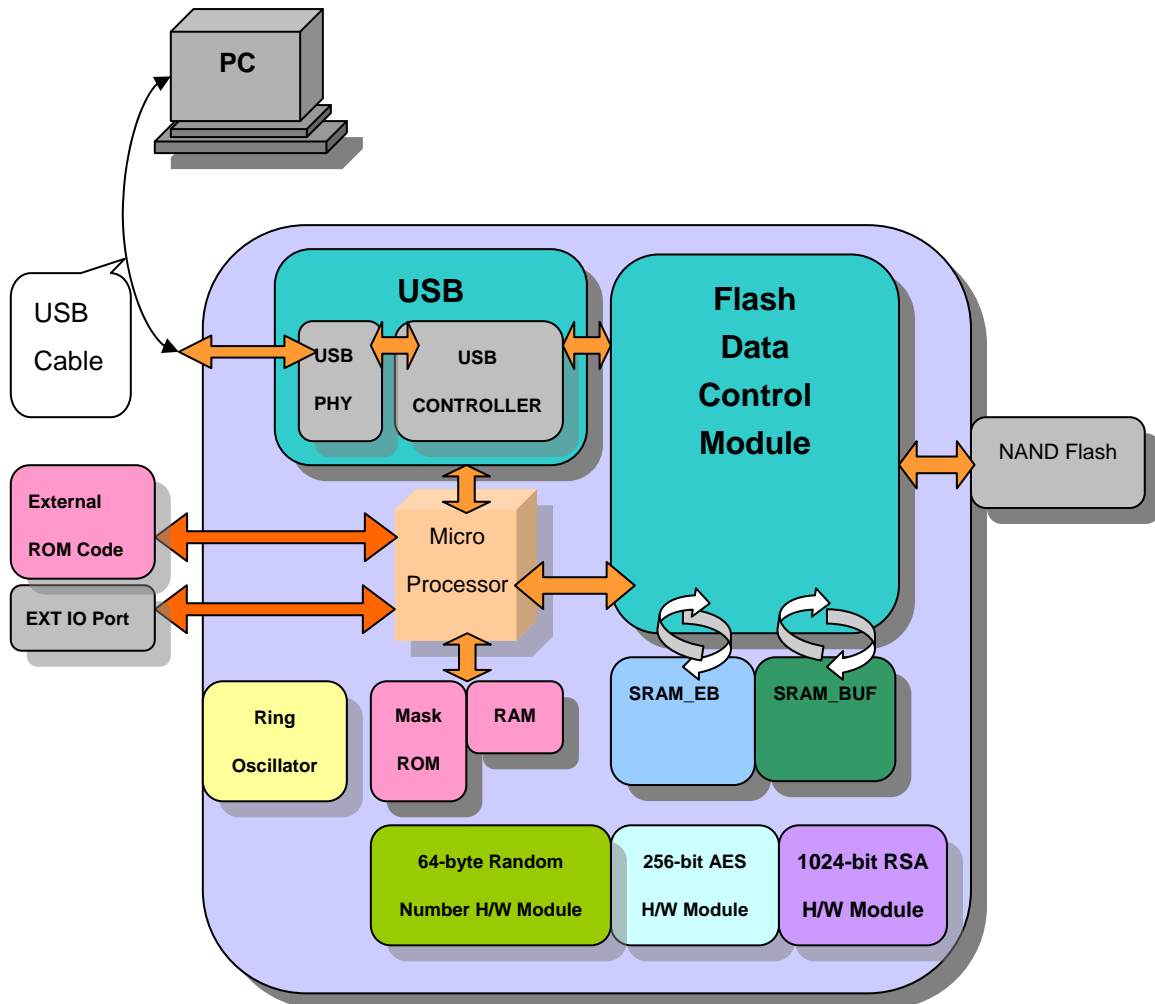
## **2 Operating Voltage: 2.7~3.6V.**

## **2 USB bus-powered capability.**

## **2 Power Saving implemented.**

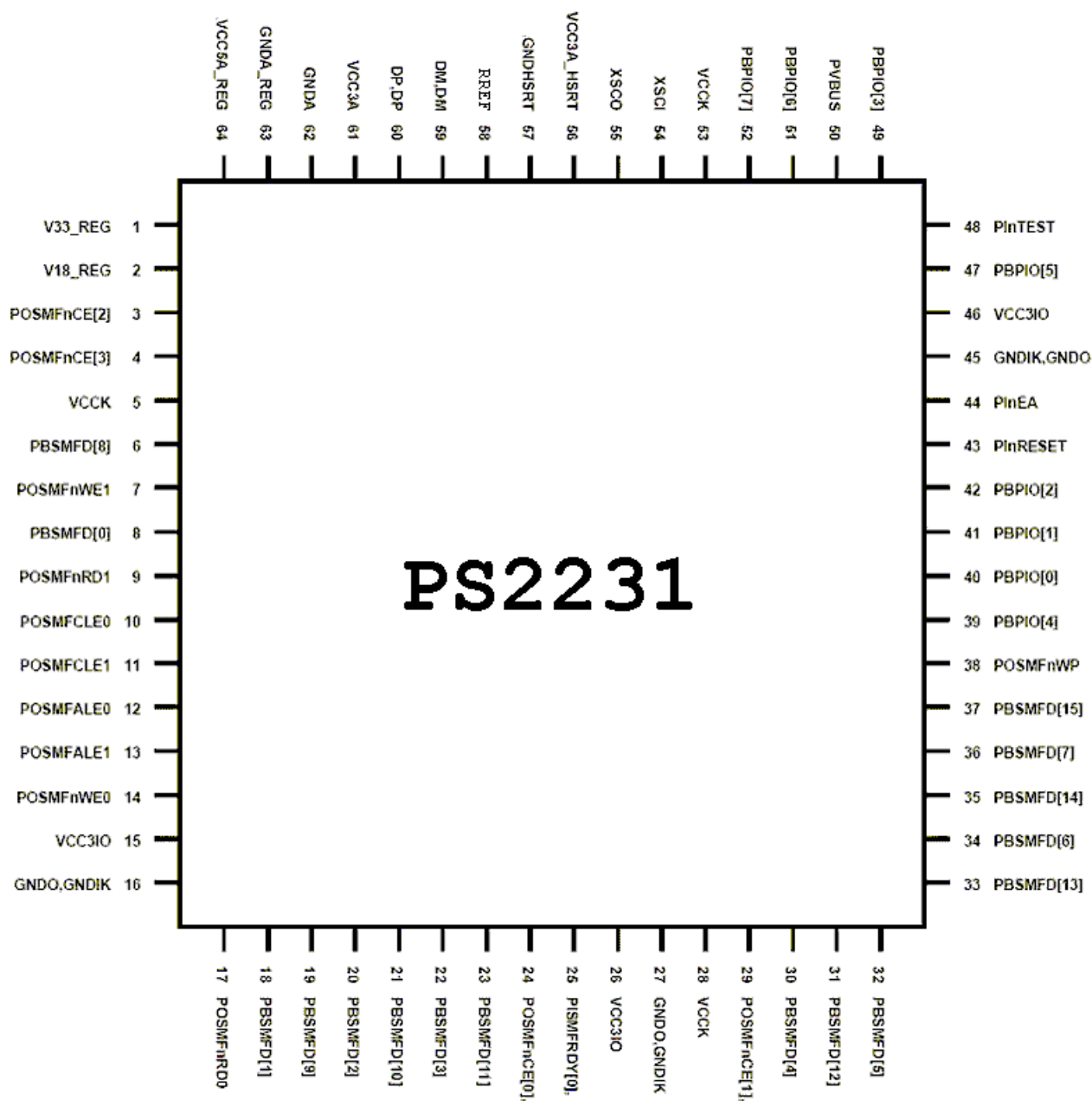
## **2 Working Frequency: 12MHz.**

## C. BLOCK DIAGRAM



## D. Pin Assignment and Description

### D1. Pin Assignment - 64pins





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## D2. Pins Listed in Numeric Order – 64pins

Pin	Signal	Pin	Signal	Pin	Signal
1	V33_REG	23	PBSMFD[11]	45	GNDIK
2	V18_REG	24	POSMF <sub>n</sub> CE[0]	46	VCC3IO
3	POSMF <sub>n</sub> CE[2]	25	PISMFRDY[0]	47	PBPIO[5]
4	POSMF <sub>n</sub> CE[3]	26	VCC3IO	48	PInTEST
5	VCKK	27	GNDO,GNDIK	49	PBPIO[3]
6	PBSMFD[8]	28	VCKK	50	PVBUS
7	POSMF <sub>n</sub> WE1	29	POSMF <sub>n</sub> CE[1]	51	PBPIO[6]
8	PBSMFD[0]	30	PBSMFD[4]	52	PBPIO[7]
9	POSMF <sub>n</sub> RD1	31	PBSMFD[12]	53	VCKK
10	POSMFCLE0	32	PBSMFD[5]	54	XSCI
11	POSMFCLE1	33	PBSMFD[13]	55	XSCO
12	POSMFALE0	34	PBSMFD[6]	56	VCC3A_HSRT
13	POSMFALE1	35	PBSMFD[14]	57	GNDHSRT
14	POSMF <sub>n</sub> WE0	36	PBSMFD[7]	58	RREF
15	VCC3IO	37	PBSMFD[15]	59	DM
16	GNDO,GNDIK	38	POSMF <sub>n</sub> WP	60	DP
17	POSMF <sub>n</sub> RD0	39	PBPIO[4]	61	VCC3A
18	PBSMFD[1]	40	PBPIO[0]	62	GNDA
19	PBSMFD[9]	41	PBPIO[1]	63	GNDA_REG
20	PBSMFD[2]	42	PBPIO[2]	64	VCC5A_REG
21	PBSMFD[10]	43	PInRESET		
22	PBSMFD[3]	44	PInEA		

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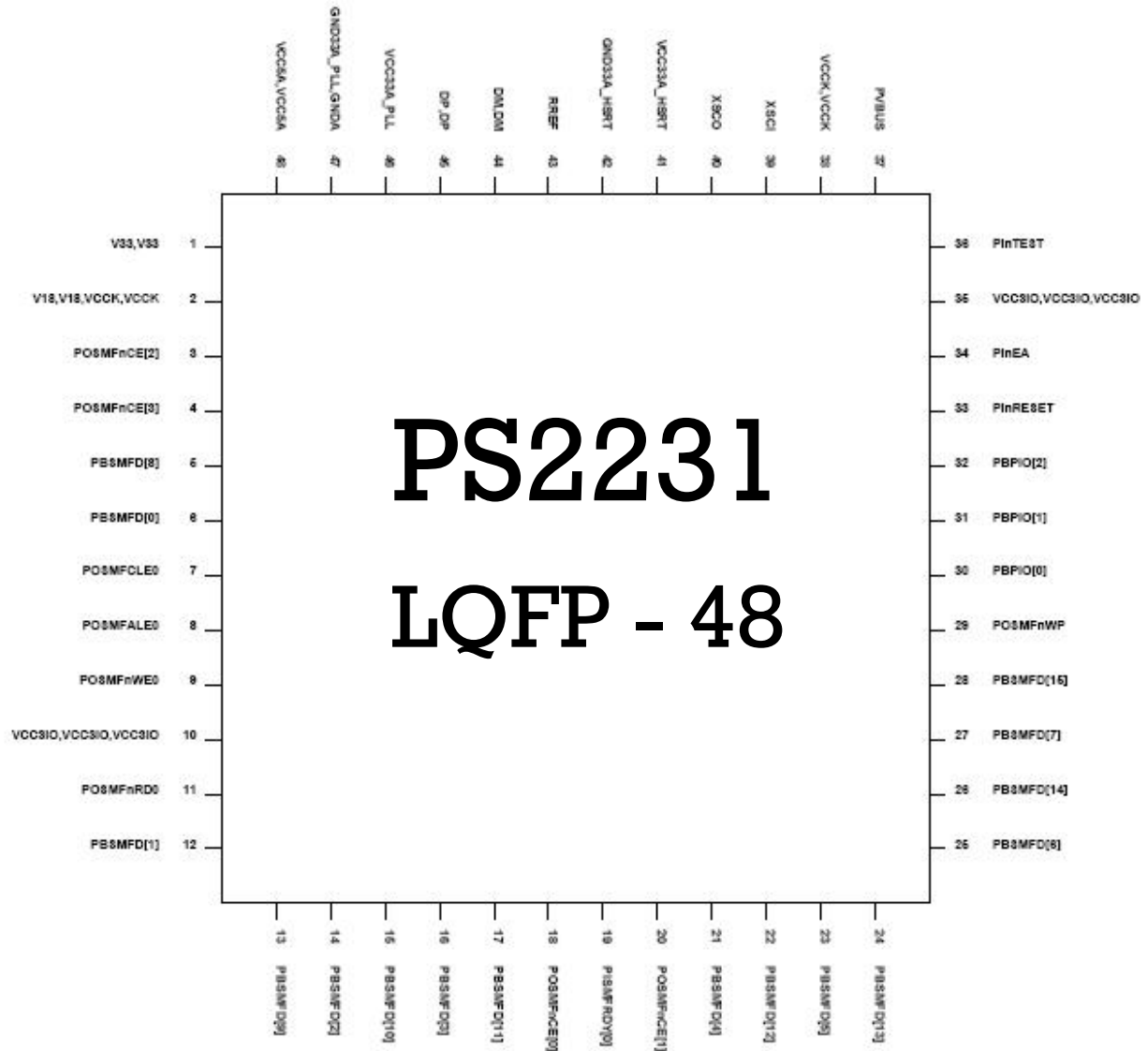
## D3. Pin Description – 64pins

USB + Regulator Interface( 13 Pins )			
No	Pin Name	Dir.	Pin Description
2	V18_REG	V18	1.8V (Regulator Digital Power output)
1	V33_REG	V33	3.3V (Regulator IO Power output)
64	VCC5A_REG	V50	5.0V
63	GNDA_REG	GND	
62	GNDA	GND	
61	VCC3A	V33	
60	DP	I/O	USB 2.0 data in positive pin terminal.
59	DM	I/O	USB 2.0 data in negative pin terminal.
58	RREF	I	For reference current. Connect it to 12.1K ohm.
57	GNDHSRT	GND	
56	VCC3A_HSRT	VCC	
55	XSCO	O	Crystal oscillator output.
54	XSCI	I	Crystal oscillator input.
FLASH Interface( 30 Pins )			
No	Pin Name	Dir.	Pin Description
24, 29, 3, 4	POSMFnCE[3: 0]	I/O	Flash Chip Enable, Low active.
8, 18, 20, 22, 30, 32, 34, 36, 6, 19, 21, 23, 31, 33, 35, 37	PBSMFD[15:0]	I/O	Flash Data Bus
12, 13	POSMFALE0, POSMFALE1	O	Flash Address Latch Enable, High active.
10, 11	POSMFCLE0, POSMFCLE1	O	Flash Command Latch Enable, High active.
17, 9	POSMFnRD0, POSMFnRD1	O	Flash Read Control signal, Low active.
14, 7	POSMFnWE0, POSMFnWE1	O	Flash Write Control signal, Low active.
38	POSMFnWP	I/O	Flash Write Protect Control signal, Low active.
25	PISMFRDY[0]	I	Flash Ready/Busy signal.
Global Signal( 21 Pins )			
No	Pin Name	Dir.	Pin Description
43	PinRESET	I	Reset Signal
48	PinTEST	I	Test Mode Signal.
44	PinEA	I	EAMODE Select Signal.
50	PVBUS	I	
40, 41, 42, 49, 39, 47, 51, 52	PBPIO[7:0]	I/O	8-bit GPIO, Internal use by F/W
15, 26, 46	VCC3IO	V33	3.3V (IO Power)
5, 28, 53	VCKK	V18	1.8V (Digital Power)
16, 27, 45	GNDIK, GNDO	GND	

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## D4. Pin Assignment - 48pins



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## D5. Pins Listed in Numeric Order – 48pins

Pin	Signal	Pin	Signal	Pin	Signal
1	V33	17	PBSMFD[11]	33	PInRESET
2	V18/VCK	18	POSMFnCE[0]	34	PInEA
3	POSMFnCE[2]	19	PISMFRDY[0]	35	VCC3IO
4	POSMFnCE[3]	20	POSMFnCE[1]	36	PInTEST
5	PBSMFD[8]	21	PBSMFD[4]	37	PVBUS
6	PBSMFD[0]	22	PBSMFD[12]	38	VCK
7	POSMFCLE0	23	PBSMFD[5]	39	XSCI
8	POSMFALE0	24	PBSMFD[13]	40	XSCO
9	POSMFnWE0	25	PBSMFD[6]	41	VCC33A_HSRT
10	VCC3IO	26	PBSMFD[14]	42	GND33A_HSRT
11	POSMFnRD0	27	PBSMFD[7]	43	RREF
12	PBSMFD[1]	28	PBSMFD[15]	44	DM
13	PBSMFD[9]	29	POSMFnWP	45	DP
14	PBSMFD[2]	30	PBPIO[0]	46	VCC33A_PLL
15	PBSMFD[10]	31	PBPIO[1]	47	GND33A_PLL/GNDA
16	PBSMFD[3]	32	PBPIO[2]	48	VCC5A

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## D6. Pin Description – 48pins

USB + Regulator Interface			
No.	Pin Name	Dir.	Pin Description
2	V18	VCC18	1.8V regulator power supply
1	V33	VCC33	3.3V regulator power supply
48	VCC5A	VCC5	5.0V regulator power input
47	GNDA	GND	0V regulator ground reference input
45	DP	I/O	USB 2.0 data in positive pin terminal.
44	DM	I/O	USB 2.0 data in negative pin terminal.
43	RREF	I	Connect to external reference resistor(12K±1%) to GND.
41	VCC33A_HSRT	VCC33	USB 2.0 IO power (3.3V)
42	GND33A_HSRT	GND	USB 2.0 IO ground reference (0V)
46	VCC33A_PLL	VCC33	USB 2.0 PLL power (3.3V)
47	GND33A_PLL	VCC33	USB 2.0 PLL ground (0V)
40	XSCO	O	Crystal oscillator output
39	XSCI	I	Crystal oscillator input
38	VCCK	I	USB 2.0 core power (1.8V)
FLASH Interface			
No.	Pin Name	Dir.	Pin Description
3,4,18,20	POSMFnCE[3:0]	O	Flash chip enable, low active.
5,6,28,27,26,25,24,23,22,21,17,16,15,14,13,12	PBSMFD[15:0]	I/O	Flash data bus
8	POSMFALE0	O	Flash address latch enable, high active.
7	POSMFCLE0	O	Flash command latch enable, high active.
11	POSMFnRD0	O	Flash read control signal, low active.
9	POSMFnWE0	O	Flash write control signal, low active.
29	POSMFnWP	O	Flash write protect control signal, low active.
19	PISMFRDY[0]	I	Flash ready/busy signal input
Global Signal			
No.	Pin Name	Dir.	Pin Description
33	PInRESET	I	Reset Signal
36	PInTEST	I	Test Mode Signal.
34	PInEA	I	EAMODE Select Signal.
37	PVBUS	I	USB VBUS input
30,31,32	PBPIO[2:0]	I/O	3-bit GPIO, Internal use by F/W
10,35	VCC3IO	VCC33	3.3V IO power
2,38	VCCK	VCC18	1.8V digital core power

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## E. System Power Consumption

Item	Power Consumption (mA)	
	1 * Flash	2 * Flash
Normal	66.00	67.03
Suspend	0.38	0.39
Sleep	0.38	0.38
Read	91.08	104.12
Write	93.88	118.74
Un-configured	42.24	42.46

The above values are for reference only, it may change according to the flash memory used.

## F. Electrical Specifications

### Absolute Maximum Rating

Item	Symbol	Parameter	MIN	MAX	Unit
1	$V_{DD}-V_{SS}$	DC Power Supply	-0.3	+5.5	V
2	$V_{IN}$	Input Voltage	$V_{SS}-0.3$	$V_{DD}+0.3$	V
3	$T_a$	Operating Temperature	0	+70	°C
4	$T_{st}$	Storage Temperature	-40	+85	°C

Parameter	Symbol	Min	Typ	MAX	Unit
Operating Temperature	$T_a$	0	+25	+70	°C
$V_{DD}$ Voltage	$V_{DD}$	3.0	3.3	3.6	V
		4.5	5.0	5.5	V

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## G. DC Characters

### DC characteristics of 3.3V I/O Cells

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
V <sub>CK</sub>	Core Power Supply	Core Area	1.62	1.8	1.98	V
V <sub>CC3IO</sub>	Power Supply	3.3V I/O	3.0	3.3	3.6	V
Temp	Junction Temperature		0	25	115	°C
V <sub>t</sub>	Switching threshold	LVTTL		1.5		V
V <sub>t-</sub>	Schmitt Trigger Negative Going threshold voltage	LVTTL	0.8	1.1		V
V <sub>t+</sub>	Schmitt Trigger Positive Going threshold voltage			1.6	2.0	V
V <sub>ol</sub>	Output Low voltage	I <sub>ol</sub>   = 2 ~ 16 mA			0.4	V
V <sub>oh</sub>	Output High voltage	I <sub>oh</sub>   = 2 ~ 16 mA	V <sub>CC3IO</sub> - 0.4			V
R <sub>pu</sub>	Input Pull-Up Resistance	PU=high, PD=low	40	75	190	KΩ
R <sub>pd</sub>	Input Pull-Down Resistance	PU=high, PD=low	40	75	190	KΩ
I <sub>in</sub>	Input Leakage Current	V <sub>in</sub> = V <sub>CC3I</sub> or 0			1	μA
I <sub>oz</sub>	Tri-state Output Leakage Current		-10	±1	10	μA

## H. AC Characters

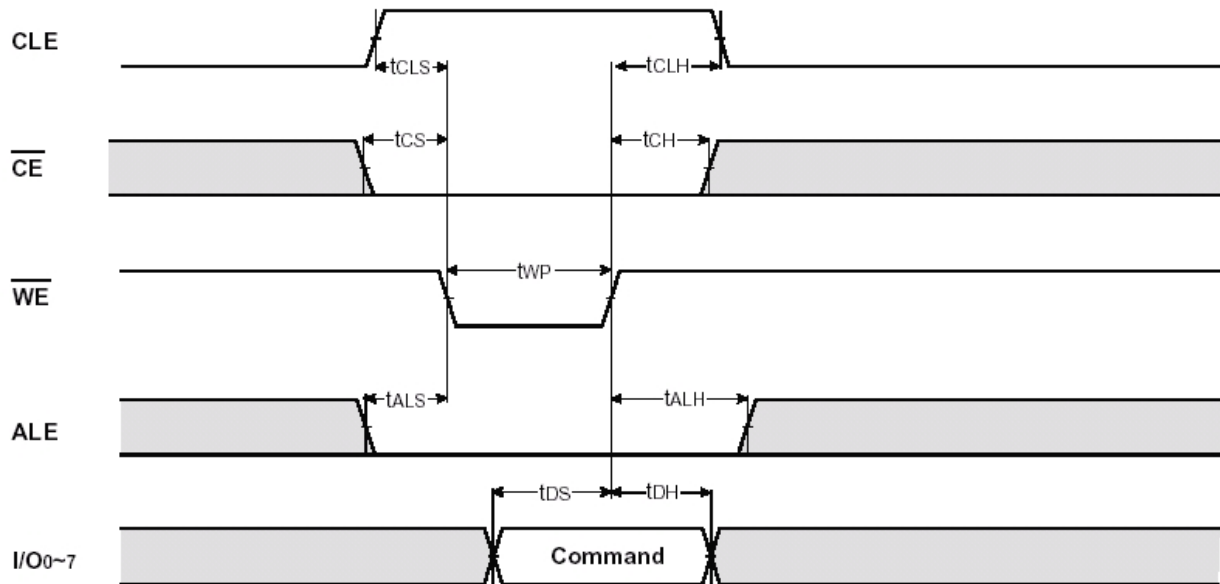
### H1. Flash Memory Interface Timing

#### *NAND Flash Memory Interface Timing*

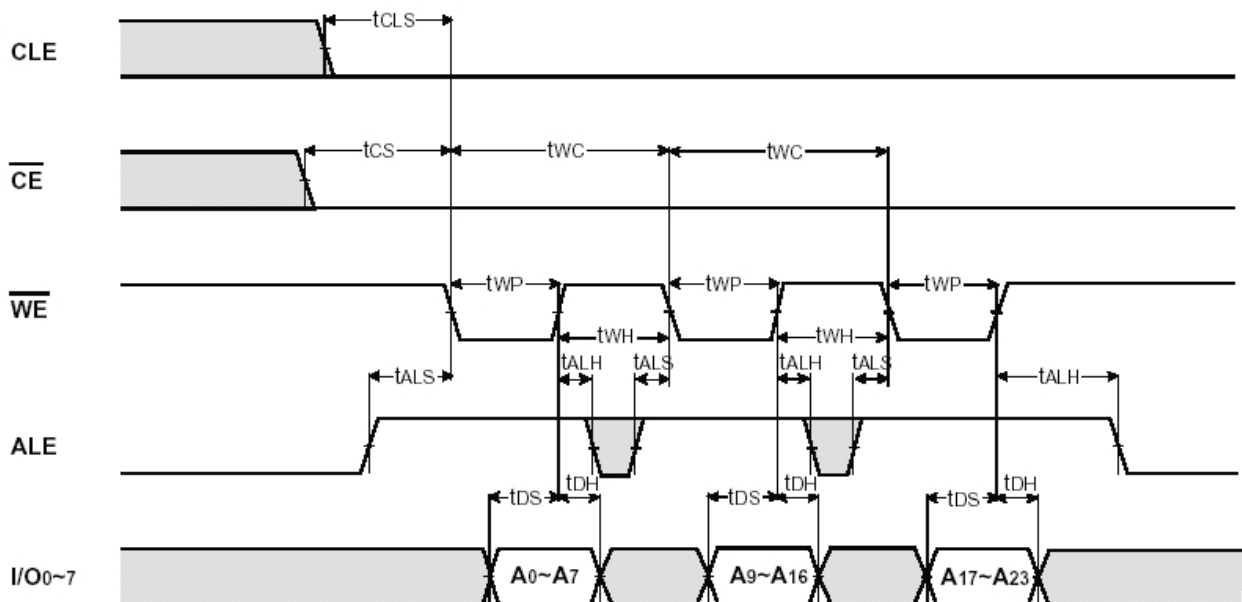
Parameter	Symbol	Min	Max	Unit
CLE Set-up Time	t <sub>CLS</sub>	0	-	ns
CLE Hold Time	t <sub>CLH</sub>	10	-	ns
CE Setup Time	t <sub>CS</sub>	0	-	ns
CE Hold Time	t <sub>CH</sub>	10	-	ns
WE Pulse Width	t <sub>WP</sub>	25	-	ns
ALE Setup Time	t <sub>ALS</sub>	0	-	ns
ALE Hold Time	t <sub>ALH</sub>	10	-	ns
Data Setup Time	t <sub>DS</sub>	20	-	ns
Data Hold Time	t <sub>DH</sub>	10	-	ns
Write Cycle Time	t <sub>WC</sub>	45	-	ns
WE High Hold Time	t <sub>WH</sub>	15	-	ns
Read Cycle Time	t <sub>RC</sub>	50	-	ns
/RE Pulse Width	t <sub>RP</sub>	25	-	ns
/RE High Hold Time	t <sub>REH</sub>	15	-	ns
Ready to /RE Low	t <sub>RR</sub>	60	-	ns



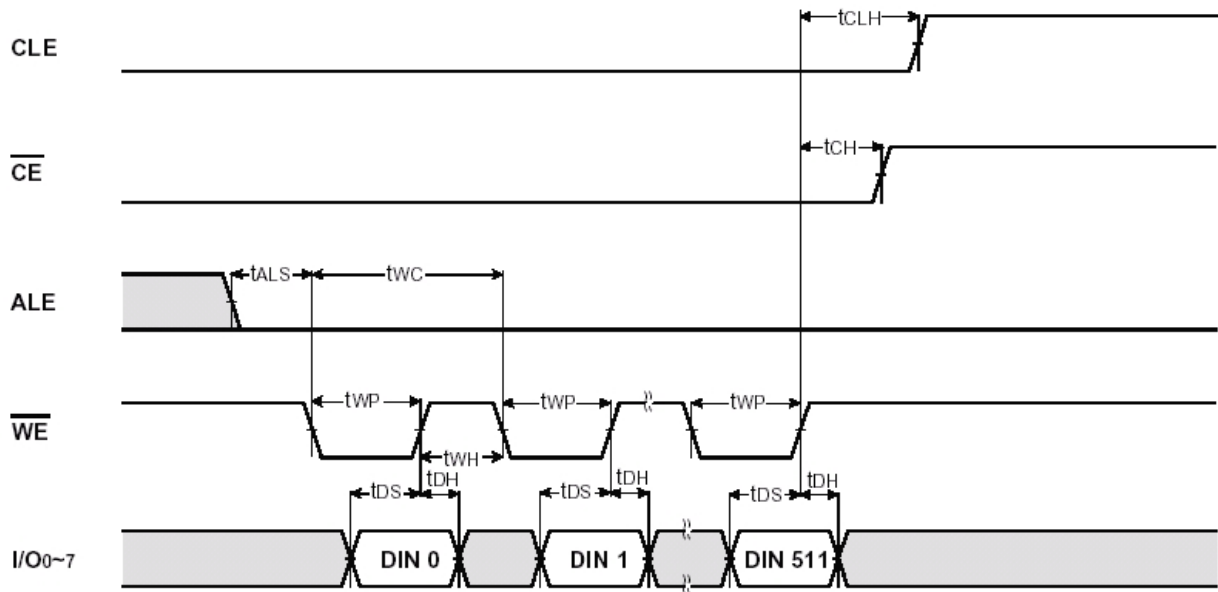
## H1.1 Command Latch Cycle



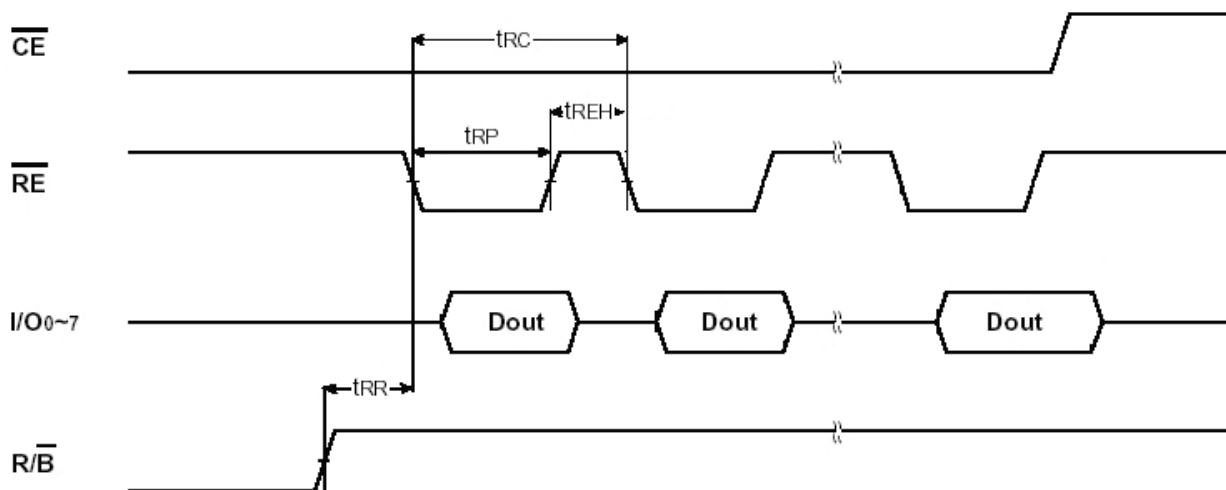
## H1.2 Address Latch Cycle



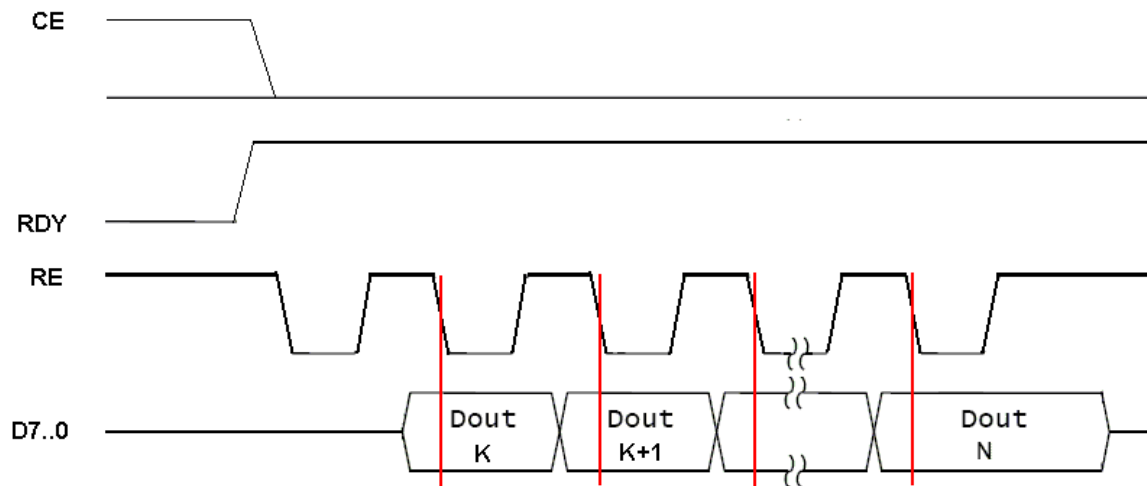
## H1.3 Input Data Latch Cycle



## H1.4 Sequential Out Cycle after Read (CLE=L, $\overline{WE}$ =H, ALE=L)





## H1.5 EDO mode for data latch

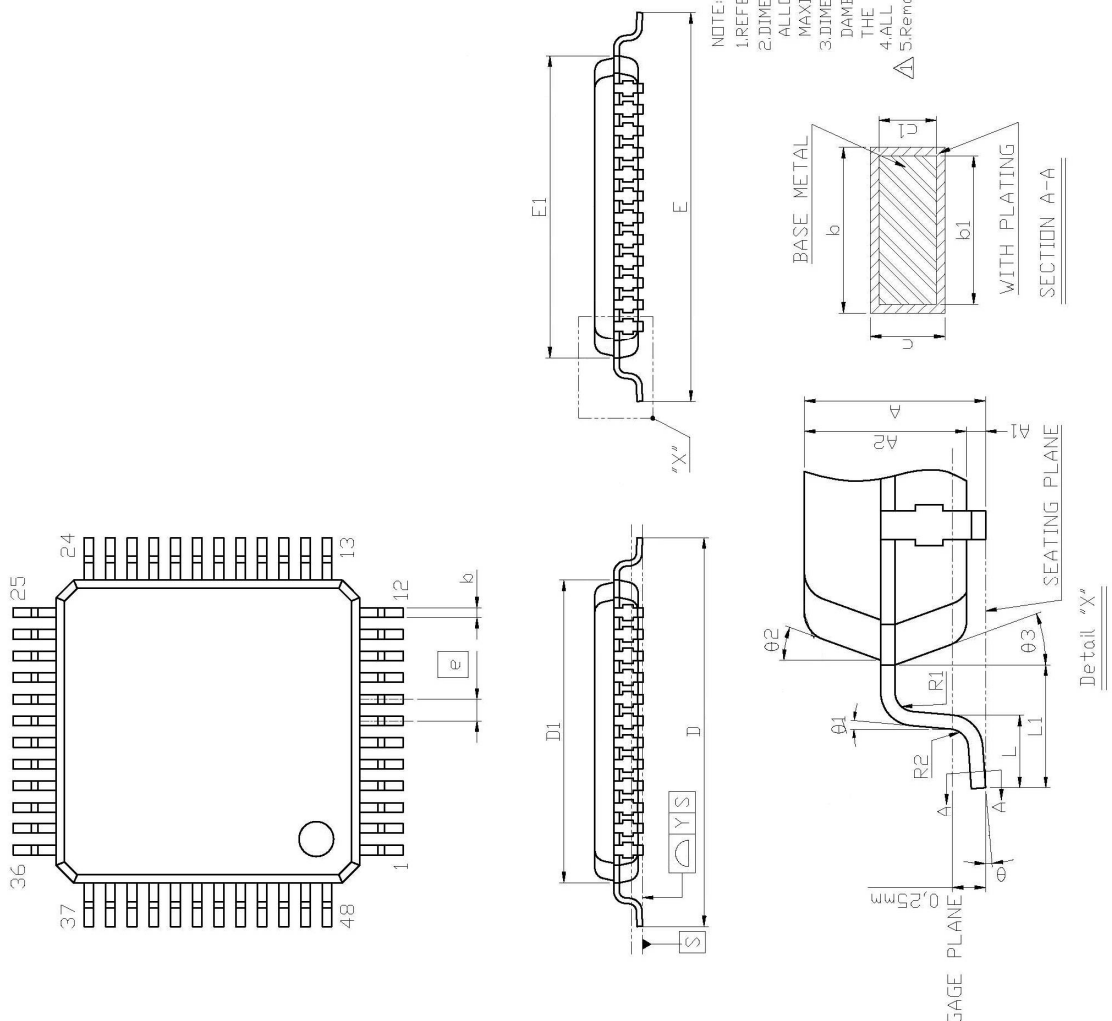


EDO mode to latch the data at the negative edge of RE.

## I1. 48 Pins

DATE	TIME	BY	REMARKS
10/10/2024	10:30	103	<p>NOTE:</p> <p>1.REFER TO JEDEC MS-026/BBC</p> <p>2.DIMENSION D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSION INCLUDING MOLD MISMATCH.</p> <p>3.DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM B DIMENSION BY MORE THAN 0.08mm.</p> <p>4.ALL DIMENSIONS IN MILLIMETERS.</p> <p>Remark:Modify PKG. CODE</p>

TITLE	LQFP48 (7x7mm)		 
	PACKAGE OUTLINE Footprint 2.0mm		
SCALE	10 : 1	PROJ.	
SHEET	1 OF 1		



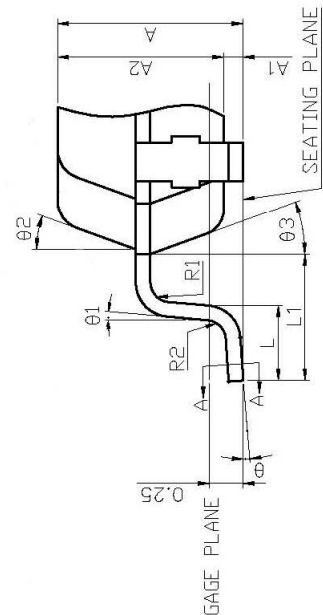
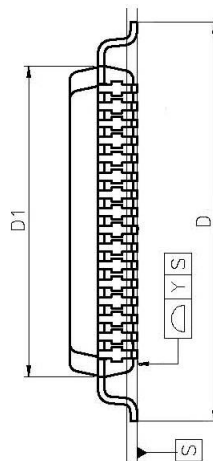
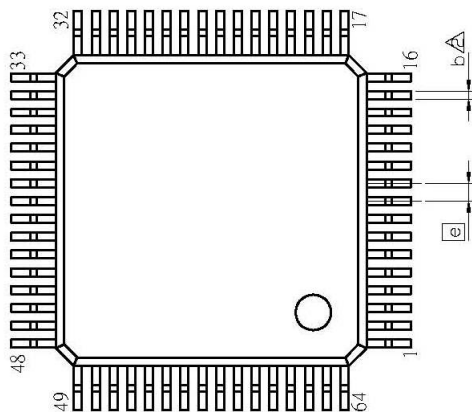
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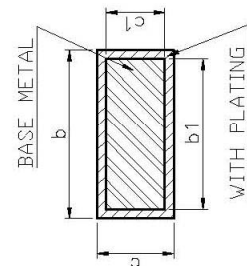
## 12. 64 Pins

SYMBOL	DIMENSION (MM)			DIMENSION (MIL)		
	MIN.	NDM.	MAX.	MIN.	NDM.	MAX.
A			1.60			63
A1	0.05		0.15	2		6
A2	1.35	1.40	1.45	53	55	57
b	0.13	0.18	0.23	5	7	9
b1	0.13	0.16	0.19	5	6	8
c	0.09		0.20	4		8
c1	0.09		0.16	4		6
D	9.00 BSC			354 BSC		
D1	7.00 BSC			276 BSC		
E	9.00 BSC			354 BSC		
E1	7.00 BSC			276 BSC		
e	0.40 BSC			15.8 BSC		
L	0.45	0.60	0.75	18	24	30
L1	1.00 REF			39 REF		
R1	0.08			3		
R2	0.08		0.20	3		8
Y			0.10			4
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°			0°		
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°

NOTE:  
1.REFER TO JEDEC MS-026(ISSUE C)/BBD  
2.DIMENSION D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION.  
ALLOWABLE PROTRUSION IS 0.25mm PER SIDE D1 AND E1 ARE  
MAXIMUM PLASTIC BODY SIZE DIMENSION INCLUDING MOLD MISWITCH.  
3.DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION, ALLOWABLE  
DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED  
THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm.  
4.ALL DIMENSIONS IN MILLIMETERS.



DETAIL "X"



SECTION A-A

TITLE LQFP64 (7x7x1.4mm)  
PACKAGE OUTLINE  
Footprint 2.0mm

SCALE 10 : 1  
SHEET 1 OF 1

