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IT1168TE

High Speed 4 Channel USB2.0 Flash Controller

Preliminary Specification V0.5

ITE TECH. INC.

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Revision History

Section	Revision	Page No.
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Order Information	<ul style="list-style-type: none">• Revised order information format	17
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1. Features

■ Spec Compliance

- High speed USB2.0 interface
- Backward compatible to USB1.1
- Integrated USB2.0 Transceiver Macrocell Interface (UTMI) and Serial Interface Engine (SIE)

■ ISP

- Support firmware ISP function to upgrade firmware

■ Enhanced Hardware Monitor

- Support four channels 8-bit flash
- Support up to 16 flash connection
- Support advanced ECC algorithm from 14 bit per 512B to 30 bit per 1KB hardware BCH ECC

■ Flash Support

- Support SLC/MLC flash
- Support 2K byte/page, 4K byte/page and 8K byte/page flash architecture with multi-channel support
- Support 2 plane operation
- Support Samsung / Hynix / Intel / Micron / PFC / Toshiba / STM flash / SMIC latest flash spec.
- Support interleave mode to accelerate read/write performance
- Support ONFI2.0 flash spec. & DDR mode access
- Support 1.8/3.3V flash

■ Multi Partition with Proprietary Tool

- One Read-Only partition is designated for Auto-Run feature
- One or two public partitions with or without security partition
- One public partition plus Auto-Run feature with or without security partition
- Security partition can be protected by password
- Capacity configuration of each partition can be done while factory initialization or by accompanied utility

■ Hardware Write-Protect Switch for Security Purpose

- Integrated 5V to 3.3V/1.8V voltage regulator to provide 3.3V for pad and 1.8 V for core operation

■ Customized VID/PID and Serial Number

- Windows 2000/XP/Vista/7, Mac 9.x above and Linux kernel 2.4 above Compatible

- LED indicator to show three different access status, Busy, Waiting, and Off

■ Package

- TQFP 64 pin

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2. General Description

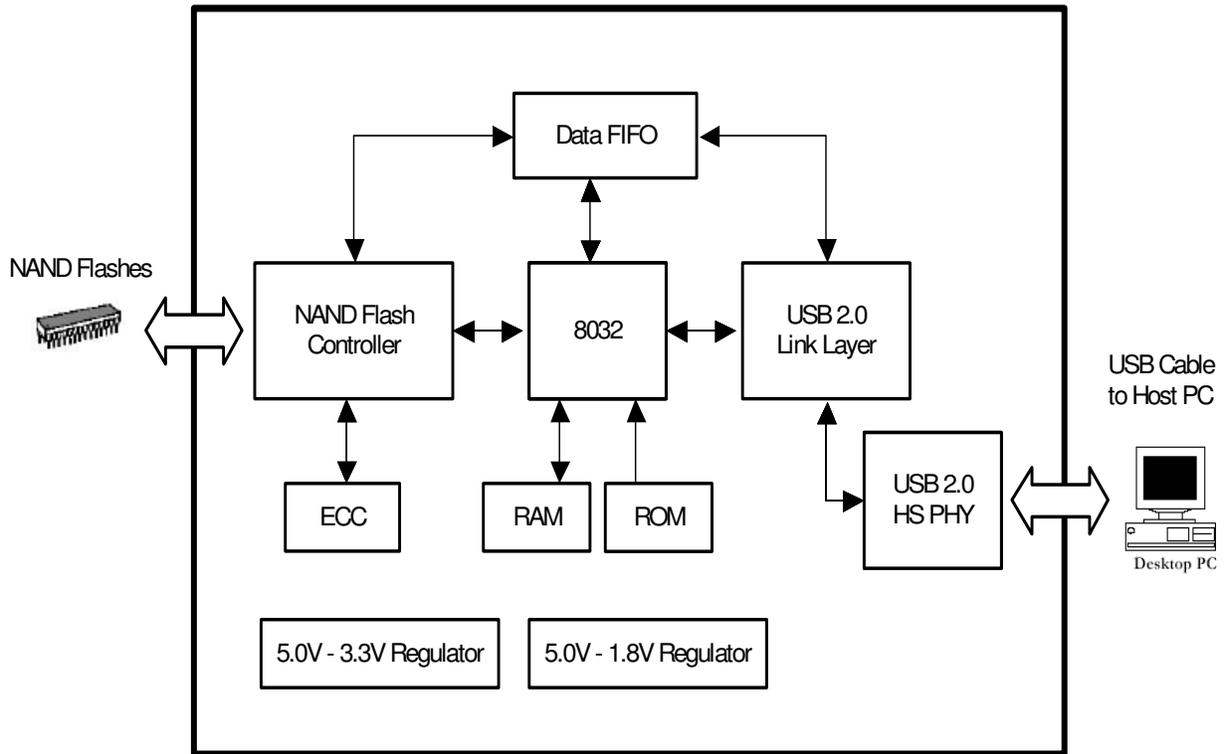
IT1168 leverages the state-of-art flash control technology to achieve extremely high performance with all types of flash technology with the unique 4 independent channels design. With 4 independent channels, not only general read/programming performance maximizes USB2.0 bandwidth but also provides the cutting-edge flash bad block management without suffering capacity lost due to high bad blocks count.

As a legacy tradition from iTE flash controllers, IT1168 broadens customers' flash selection by its industry-leading 30 bit hardware ECC engine, which remains customers more competitive on latest flash technology, including Hynix 41nm/Samsung 35nm/IM 34nm/Toshiba 43nm or more advanced, either MLC or TLC specification. Further more, IT1168 completes ONFI2.0 design on DDR type flash support to create end product difference in terms of performance and reliability.

Differed from previous generic designs, propelling new flash interleave algorithm and flash management with efficiency-oriented independent channel design on firmware design, that IT1168 sets up a new challenging mantra to last generation products.

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3. Block Diagram



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5. Pin Description

Table 5-1 TQFP 64 Pin Description

Pin	Signal	Attribute	Description	Pin	Signal	Attribute	Description
● 1	REG18V	P	Regulator 1.8V power out	33	F1_IO0	IO	Group1, flash data bus 0
● 2	REG33V	P	Regulator 3.3V power out	34	F1_IO1	IO	Group1, flash data bus 1
● 3	F3_IO4	IO	Group3, flash data bus 4	35	F1_IO2	IO	Group0, flash data bus 2
● 4	F3_IO3	IO	Group3, flash data bus 3	36	F1_IO3	IO	Group1, flash data bus 0
● 5	F3_IO2	IO	Group3, flash data bus 2	37	F1_IO4	IO	Group1, flash data bus 4
● 6	F3_IO1	IO	Group3, flash data bus 1	38	F1_IO5	IO	Group1, flash data bus 5
● 7	F3_IO0	IO	Group3, flash data bus 0	39	F1_IO6	IO	Group1, flash data bus 6
● 8	VSS	P	Logic ground	40	F1_IO7	IO	Group1, flash data bus 7
● 9	TESTEN	I	Test enable	41	VSS	P	Logic ground
● 10	IVDD18	P	Logic 1.8V power	42	F_CE_N2	O	Flash chip enable 2 (active low)
● 11	RST_N	I	External reset pin (active low)	43	F_CE_N3	O	Flash chip enable 3 (active low)
● 12	LED_N	O	LED indication	44	F2_IO0	IO	Group2, flash data bus 0
● 13	AVDD33	P	Analog 3.3V power	45	F2_IO1	IO	Group2, flash data bus 1
● 14	DP	IO	USB Data positive pin	46	F2_IO2	IO	Group2, flash data bus 2
● 15	DM	IO	USB Data negative pin	47	F2_IO3	IO	Group2, flash data bus 3
● 16	AVSS	P	Analog ground	48	IVDD18	P	1.8V power
● 17	XTALO	O	Crystal output	49	F2_IO4	IO	Group2, flash data bus 4
● 18	XTALI	I	Crystal input	50	F2_IO5	IO	Group2, flash data bus 5
● 19	F_RB3_N	I	Flash 3 ready busy pin (active low)	51	F2_IO6	IO	Group2, flash data bus 6
● 20	F_RB2_N	I	Flash 2 ready busy pin (active low)	52	F2_IO7	IO	Group2, flash data bus 7
● 21	F3_IO6	IO	Group3, flash data bus 6	53	F0_CLE	O	Flash 0 command latch enable
● 22	F3_IO7	IO	Group3, flash data bus 7	54	F0_ALE	O	Flash 0 address latch enable
● 23	F0_IO0	IO	Group0, flash data bus 0	55	IOVDD	P	IO pin power. Upon flash source connection (3.3V or 1.8V)
● 24	F0_IO1	IO	Group0, flash data bus 1	56	VSS	P	Logic ground
● 25	F0_IO2	IO	Group0, flash	57	F_CE_N0	O	Flash chip

			data bus 2				enable 0 (active low)
● 26	F0_IO3	IO	Group0, flash data bus 3	58	F_CE_N1	O	Flash chip enable 1 (active low)
● 27	VSS	P	Logic ground	59	F_RB0_N	I	Flash 0 ready busy pin (active low)
● 28	F0_IO4	IO	Group0, flash data bus 4	60	F_RB1_N	I	Flash 1 ready busy pin (active low)
● 29	F0_IO5	IO	Group0, flash data bus 5	61	F_WE_N	O	Flash write enable (active low)
● 30	F0_IO6	IO	Group0, flash data bus 6	62	F_RE_N	O	Flash read enable (active low)
● 31	F0_IO7	IO	Group0, flash data bus 7	63	F3_IO5	IO	Group3, flash data bus 5
● 32	IOVDD	P	IO pin power. Upon flash source connection (3.3V or 1.8V)	64	REG5V	P	Regulator 5V power in

*I: input, O: output, IO: bi-direction, P: power

6. DC Characteristics

Absolute Maximum Ratings

Storage Temperature (T_{storage}).....-40°C to 85°C
Ambient Operating Temperature (Ta).....0°C to 75°C

Comments

Extended exposure to the maximum ratings might degrade device reliability. Although IT1168 has protective circuitry to resist damage from electrostatic discharge (ESD), precautions should always be taken to avoid high voltage or electric field.

Table 6-1 Absolute Maximum Ratings

Symbol	Parameter	Min.	Max.	Unit	Note
T _{storage}	Storage Temperature	-40	85	°C	-
Ta	Ambient Operating Temperature	0	75	°C	-
REG33V	3.3V Supply Voltage	-0.3	3.6	V	-
REG18V	1.8V Supply Voltage	-0.3	2	V	-
VDD33	3.3V Buffer Input Voltage	-0.3	3.6	V	-
REG5V	3.3V/5V Buffer Input Voltage	-0.3	5.5	V	-
IOVDD with 3.3V	3.3V Buffer Input Voltage	-0.3	3.6	V	-
IOVDD with 1.8V	1.8V Buffer Input Voltage	-0.3	2	V	-

Table 6-2 Operating Conditions

Symbol	Parameter	Min.	Max.	Unit
REG5V	USB 5V Supply Voltage	3.2	5.5	V
REG33V	3.3V Supply Voltage	3.0	3.6	V
REG18V	1.8V Supply Voltage	1.6	2	V

Table 6-3 DC Characteristics of I/O Interface

Symbol	Parameter	Min	Max	Unit
V _{IH_TTL}	TTL Input High Voltage	2	VDD33+0.3	V
V _{IL_TTL}	TTL Input Low Voltage	-0.3	0.8	V
V _{OH_TTL}	TTL Output High Voltage	0.9VDD33		V
V _{OL_TTL}	TTL Output Low Voltage		0.45	V
I _{OH_TTL}	TTL Output High Current	-4		mA

Symbol	Parameter	Min	Max	Unit
I _{OL_TTL}	TTL Output Low Current		4	mA
V _{IH_USB}	USB Input High Voltage for Low-/full-speed	2.0		V
V _{IL_USB}	USB Input Low Voltage for Low-/full-speed		0.8	V
V _{I_USB_DIFF}	Differential Input Sensitivity for Low-/full-speed	TBD		V
V _{I_USB_CM}	Differential Common Mode Input Range for Low-/full-speed	0.8	2.5	V
V _{I_USB_HSSQ}	USB High-speed squelch Input detection threshold	0.1	0.15	V
V _{I_USB_HSDSC}	USB High-speed disconnect Input detection threshold	0.525	0.625	V
V _{I_USB_HSCM}	USB High-speed Signaling Common Mode Range	-0.05	0.5	V
V _{OH_USB}	USB Output High Voltage for Low-/full-speed	2.8	3.6	V
V _{OL_USB}	USB Output Low Voltage for Low-/full-speed	0	0.3	V
V _{OH_USB_HS}	USB Output High Voltage for High-speed	0.36	0.44	V
V _{OL_USB_HS}	USB Output Low Voltage for High-speed	-0.01	0.01	V
I _{OH_USB}	USB Output High Current for Low-/full-speed	-10		mA
I _{OL_USB}	USB Output Low Current for Low-/full-speed		10	mA
I _{OH_USB_HS}	USB Output High Current for High-speed	-40		mA
I _{OL_USB_HS}	USB Output Low Current for High-speed		40	mA

7. AC Characteristics

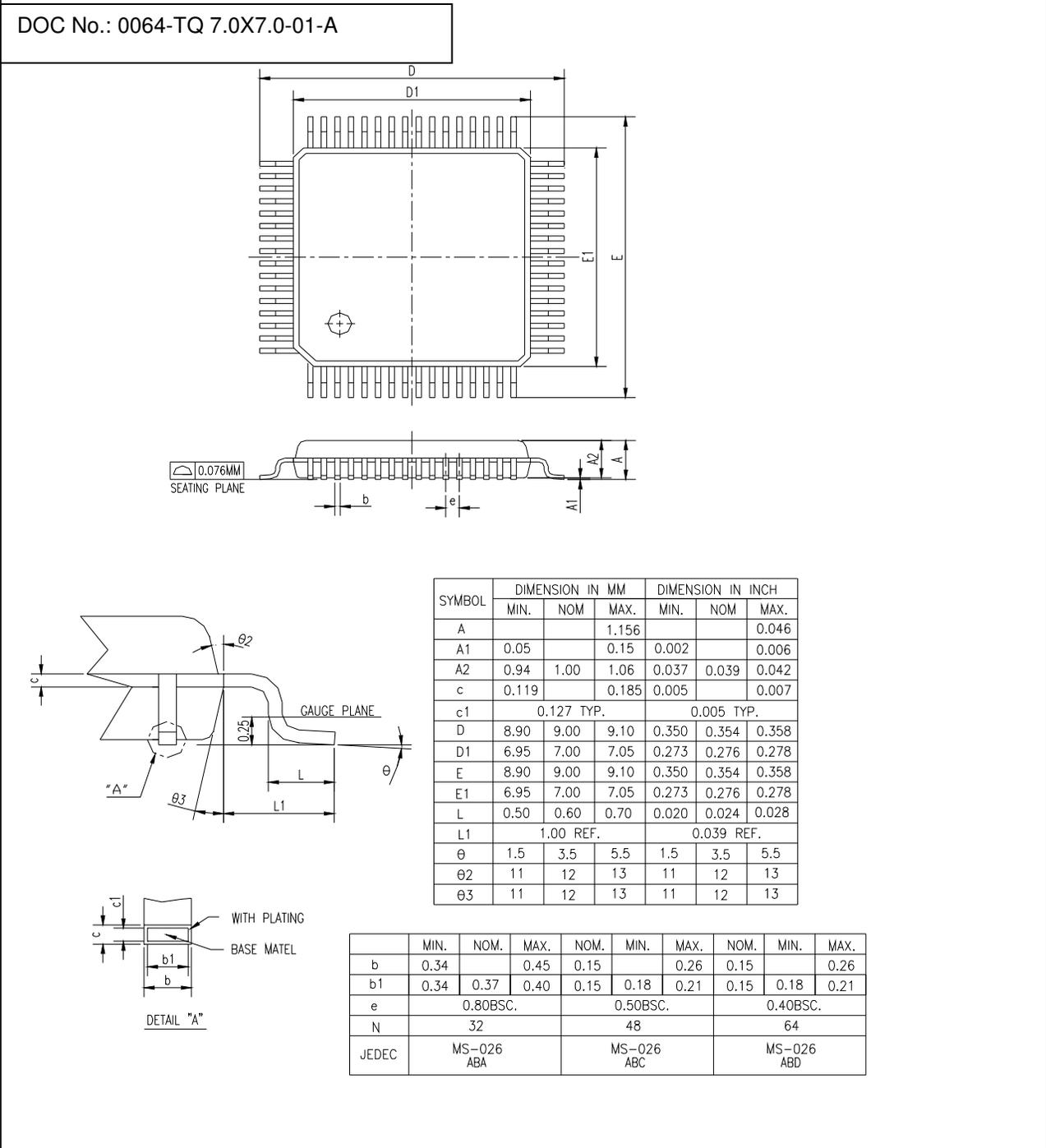
Table 7-1 AC Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit
TP _{ILH}	Input rising delay	0.61 (0.8pF)	0.72 (2.4pF)	0.92 (4.8pF)	ns
TP _{IHL}	Input falling delay	0.88 (0.8pF)	1.03 (2.4pF)	1.24 (4.8pF)	ns
TP _{OLH}	Output rising delay	2.40 (10pF)	2.768 (30pF)	4.88 (60pF)	ns
TP _{OHL}	Output falling delay	1.905 (10pF)	2.614 (30pF)	5.03 (60pF)	ns
TR	Output rising time	1.052 (10pF)	2.761 (30pF)	7.83 (60pF)	ns
TF	Output falling time	0.932 (10pF)	2.133 (30pF)	6.23 (60pF)	ns

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8. Package Information

64 TQFP Outline Dimension



64 Pin TQFP 7.0x7.0x1.0 mm Package Outline Dimension

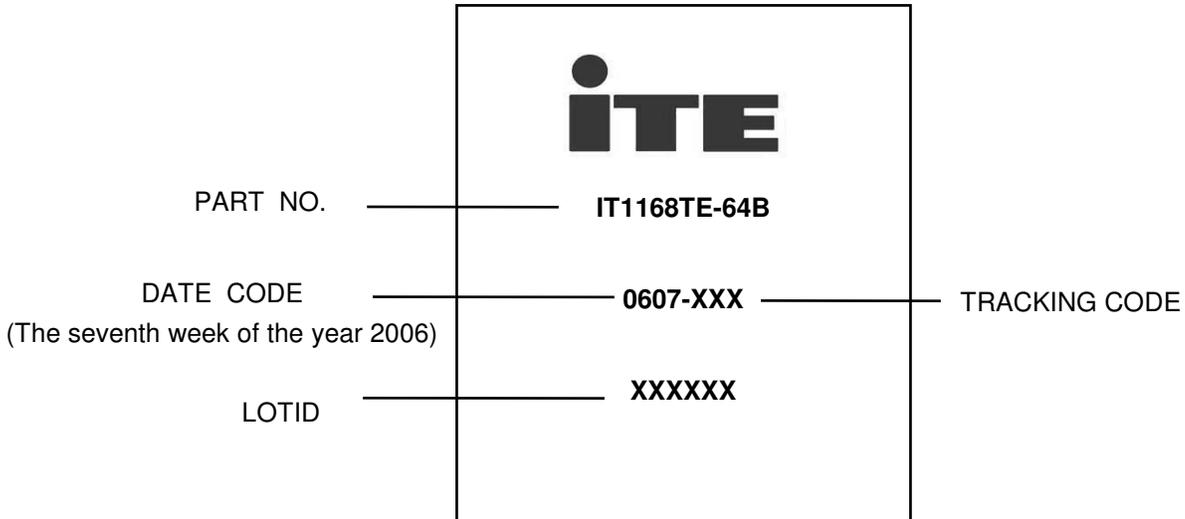
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9. Ordering Information

Part No.	Package
IT1168TE-64B/BX	TQFP 64

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10. Top Marking Information



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- Shipments are subject to availability. Seller shall make every reasonable effort to meet the date(s) quoted or acknowledged; and if Seller makes such effort, Seller will not be liable for any delays.

3. TERMS OF PAYMENT

- Terms are as stated on Seller's quotation, or if none are stated, net thirty (30) days. Accounts past due will incur a monthly charge at the rate of one percent (1%) per month (or, if less, the maximum allowed by applicable law) to cover servicing costs.
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- Goods or parts which have been subject to abuse (including without limitation repeated or extended exposure to conditions at or near the limits of applicable absolute ratings) misuse, accident, alteration, neglect, or unauthorized repair or improper application are not covered by any warranty. No warranty is made with respect to custom products or goods produced to Buyer's specifications (unless specifically stated in a writing signed by Seller).
- No warranty is made with respect to goods used in devices intended for use in applications where failure to perform when properly used can reasonably be expected to result in significant injury (including, without limitation, navigation, aviation or nuclear equipment, or for surgical implant or to support or sustain life) and Buyer agrees to indemnify, defend, and hold harmless Seller from all claims, damages and liabilities arising out of any such uses.
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9. NO CONFIDENTIAL INFORMATION

Seller shall have no obligation to hold any information in confidence except as provided in a separate non-disclosure agreement signed by both parties.

10. ENTIRE AGREEMENT

- These terms and conditions are the entire agreement and the only representations and understandings between Seller and Buyer, and no addition, deletion or modification shall be binding on Seller unless expressly agreed to in written and signed by an officer of Seller.
- Buyer is not relying upon any warranty or representation except for those specifically stated here.

11. APPLICABLE LAW

The contract and all performance and disputes arising out of or relating to goods involved will be governed by the laws of R.O.C. (Taiwan, Republic of China), without reference to the U.N. Convention on Contracts for the International Sale of Goods or to conflict of laws principles. Buyer agrees at its sole expense to comply with all applicable laws in connection with the purchase, use or sale of the goods provided hereunder and to indemnify Seller from any failure by Buyer to so comply. Without limiting the foregoing, Buyer certifies that no technical data or direct products thereof will be made available or re-exported, directly or indirectly, to any country to which such export or access is prohibited or restricted under R.O.C. laws or U.S. laws or regulations, unless prior authorization is obtained from the appropriate officials and agencies of the government as required under R.O.C. or U.S. laws or regulations.

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The courts located in Hsinchu, Taiwan, Republic of China, will have the sole and exclusive jurisdiction and venue over any dispute arising out of or relating to the contract or any sale of goods hereunder. Buyer hereby consents to the jurisdiction of such courts.

13. ATTORNEYS' FEES

Reasonable attorneys' fees and costs will be awarded to the prevailing party in the event of litigation involving and/or relating to the enforcement or interpretation of the contract and/or any goods sold under it.