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Phison Electronics Corporation

USB 2.0 Flash Controller Specification PS2251-50

Version 1.0

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Document Number : S-09050

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Revision History

Revision	History	Date
1.0	New Release	1-Sep-2009

A. General Description

The PHISON's PS2251-50 micro-controller supports USB 2.0 & 1.1 and interface to NAND Flash Memory. This chip is specially designed for portable storage device or build-in to the PC / Notebook / IA system.

PS2251-50 controller implements with PRAM (program RAM) architecture, which can upgrade firmware code anytime if required. This is very helpful for time-to-market & Mass Production solution. PS2251-50 controller is also a crystal free solution. With this crystal free solution, it will save 40% on the PCBA cost.

By using this single chip solution, it will reduce a lot of efforts which was needed from R/D to production, as well as simplifying the RMA problems. With the USB plug & play function and driver-less solution with most of the operating systems, this solution provides not only easy to install, but also fast, easy to use and low cost way for user.

B. Controller Features

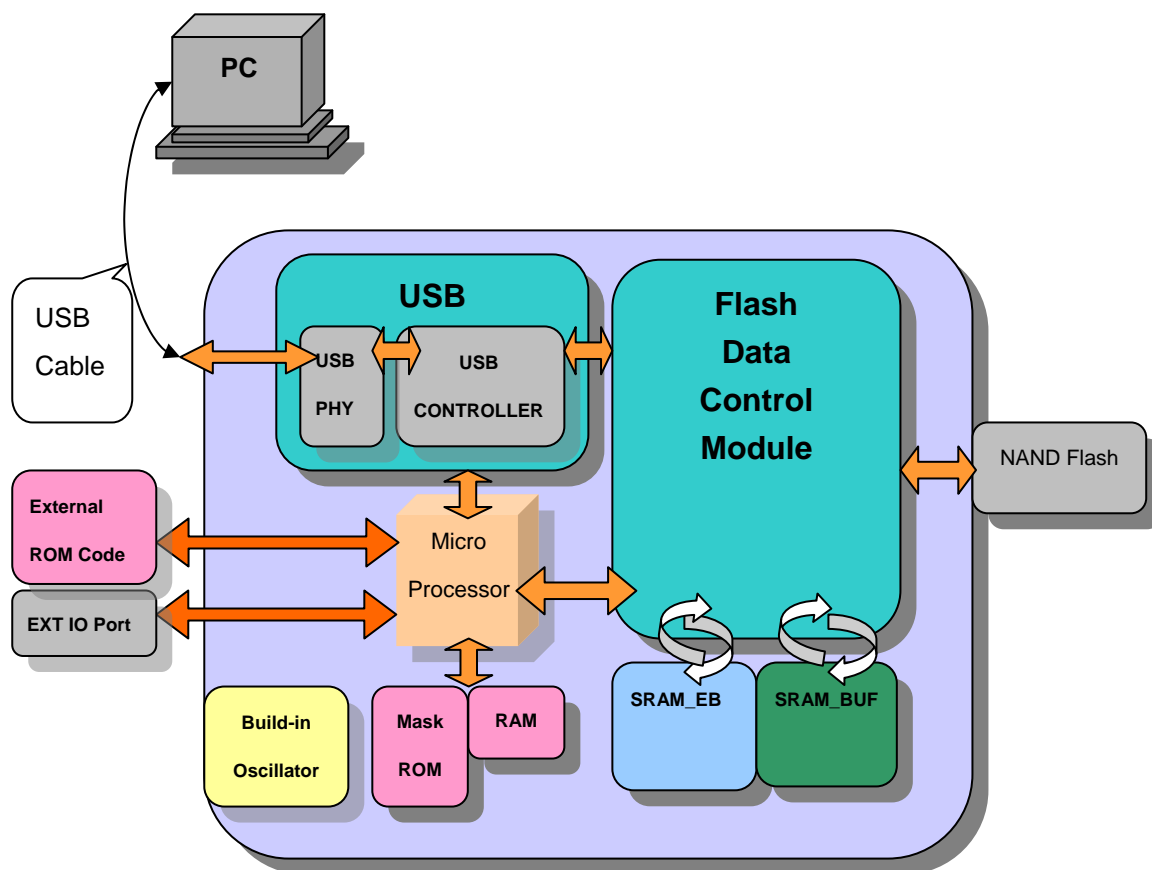
- 2 **Support Host Interfaces : USB 2.0 & 1.1 Interface**
 - Fully compatible with USB Specification Version 2.0 & 1.1
 - High speed 480Mbit/second supporting
 - Full speed 12Mbit/second supporting
 - Support one CONTROL transfer, one INTERRUPT transfer and two BULK transfer
 - Support four Endpoints :
 - Ø Endpoint 0 : 64 Bytes CONTROL transfer
 - Ø Endpoint 1 : 512 Bytes BULK transfer for IN transaction
 - Ø Endpoint 2 : 512 Bytes BULK transfer for OUT transaction
 - Ø Endpoint 3 : 64 Bytes INTERRUPT transfer for IN transaction
 - Support Data Payload
 - Ø Endpoint 0 : max 64 bytes
 - Ø Endpoint 1 : max 512 bytes
 - Ø Endpoint 2 : max 512 bytes
 - Ø Endpoint 3 : max 64 bytes
 - Support USB power saving mode
- 2 **Build-In NAND Flash Memory Interface**
 - Build-in hardware ECC circuit.
 - Support SLC (Single level cell) 4k-page large block NAND Flash.
 - Support MLC (Multi level cell) 4k-page Large Block NAND flash.
 - Support MLC (Multi level cell) 8k-page Large Block NAND flash.
- 2 **Support 3.3V Flash I/O:**

Internal 3.3V regulator can supply current for controller analog circuit, controller I/O and Flash.
- 2 **Support 1.8V Flash I/O:**

Internal 1.8V regulator can supply the current for controller core, controller I/O and Flash.

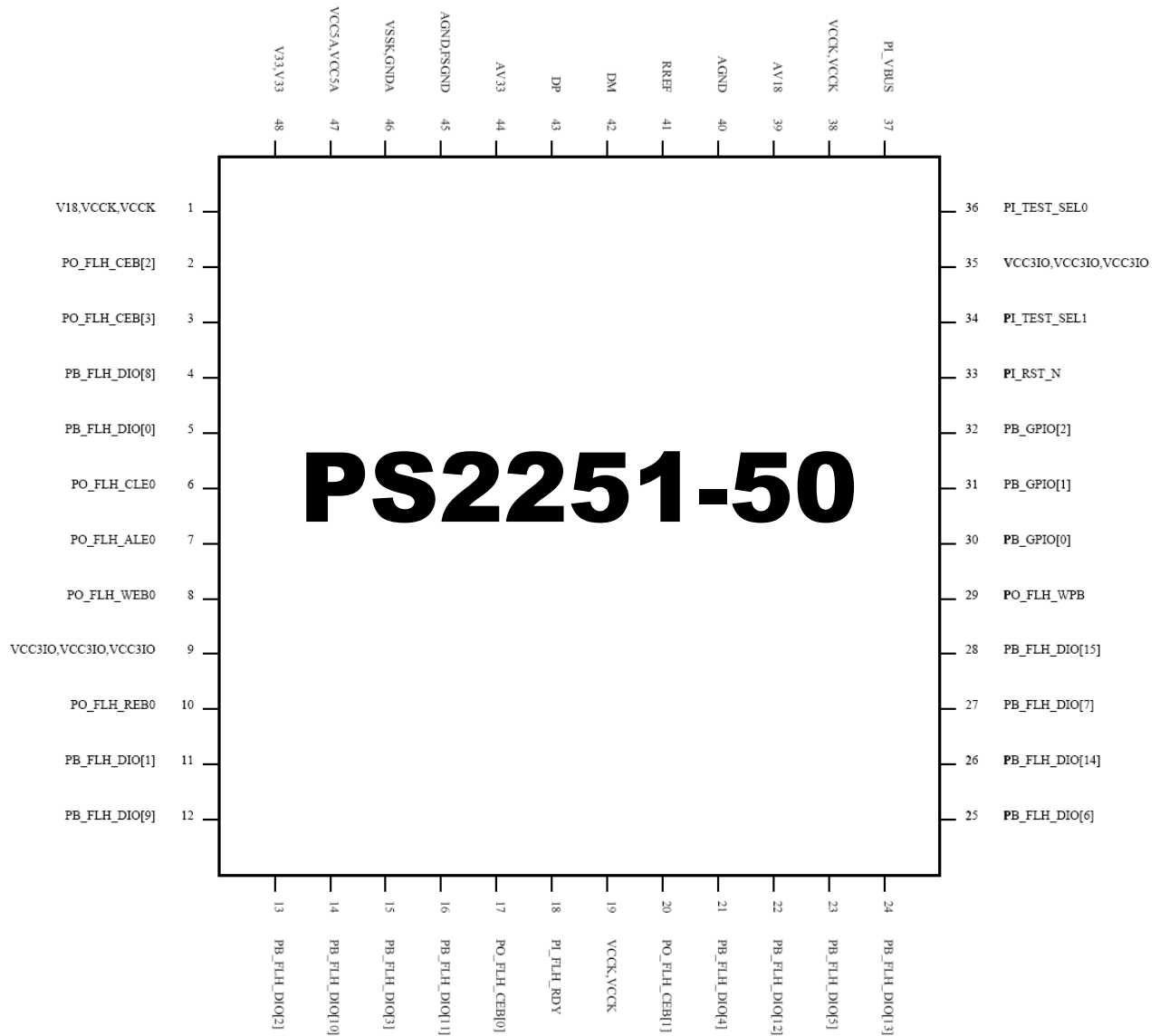
- 2 **Support In-System Programming through USB Port**
- 2 **Buffer SRAM :** 32 buffers for performance improvement
- 2 **Build-in regulator**
- 2 **Crystal free solution**
- 2 **48-pins QFP Package**
- 2 **Operating Voltage:** 4.5V ~ 5.5V.
- 2 **USB bus-powered capability.**
- 2 **Power Saving implemented.**

C. BLOCK DIAGRAM



D. Pin Assignment and Description

D1. Pin Assignment - 48pins



D2. Pins Listed in Numeric Order – 48pins

Pin	Signal	Pin	Signal	Pin	Signal
1	V18,VCCK,VCCK	17	PO_FLH_CEB[0]	33	PI_RST_N
2	PO_FLH_CEB[2]	18	PI_FLH_RDY	34	PI_TEST_SEL1
3	PO_FLH_CEB[3]	19	VCCK,VCCK	35	VCC3IO
4	PB_FLH_DIO[8]	20	PO_FLH_CEB[1]	36	PI_TEST_SELO
5	PB_FLH_DIO[0]	21	PB_FLH_DIO[4]	37	PI_VBUS
6	PO_FLH_CLE0	22	PB_FLH_DIO[12]	38	VCCK,VCCK
7	PO_FLH_ALE0	23	PB_FLH_DIO[5]	39	AV18
8	PO_FLH_WEB0	24	PB_FLH_DIO[13]	40	AGND
9	VCC3IO	25	PB_FLH_DIO[6]	41	RREF
10	PO_FLH_REB0	26	PB_FLH_DIO[14]	42	DM
11	PB_FLH_DIO[1]	27	PB_FLH_DIO[7]	43	DP
12	PB_FLH_DIO[9]	28	PB_FLH_DIO[15]	44	AV33
13	PB_FLH_DIO[2]	29	PO_FLH_WPB	45	AGND,FSGND
14	PB_FLH_DIO[10]	30	PB_GPIO[0]	46	VSSK,GNDA
15	PB_FLH_DIO[3]	31	PB_GPIO[1]	47	VCC5A,VCC5A
16	PB_FLH_DIO[11]	32	PB_GPIO[2]	48	V33,V33

D3. Pin Description

USB + Power Interface		
Pin Name	Dir.	Pin Description
VCC5A	VCC	5.0V regulator power supply
V33	VCC	3.3V regulator power supply
V18	VCC	1.8V regulator power supply
GND A	GND	0.0V regulator ground
VDET	VCC	voltage detector
AVDDH_USB	VCC	3.3V USB power supply
AGND_USB	GND	0.0V USB ground
AVDDHP	VCC	3.3V USB power supply
AGNDP	GND	0.0V USB ground
NC	-	No Connection
DP	I/O	USB positive pin terminal
DM	I/O	USB negative pin terminal

FLASH Interface		
Pin Name	Dir.	Pin Description
PB_FLH_DIO[15:0]	I/O	Flash data bus
PO_FLH_CEB[3:0]	O	Flash chip enable, low active.
PI_FLH_RDY	I	Flash ready/busy signal input
PO_FLH_WPB	O	Flash write protect control signal
PO_FLH_REB0	O	Flash read control signal
PO_FLH_WEB0	O	Flash write control signal
PO_FLH_ALE0	O	Flash address latch enable
PO_FLH_CLE0	O	Flash command latch enable

Global Signal		
Pin Name	Dir.	Pin Description
PI_RST_N	I	Reset Signal
PI_VBUS	I	USB VBUS input
PI_TEST_SEL0	I	Test Mode Signal
PI_TEST_SEL1	I	Test Mode Signal
XSCO	O	Crystal oscillator output
XSCI	I	Crystal oscillator input
PB_GPIO[2:0]	I/O	General purpose I/O

E. System Power Consumption

Item	Power Consumption (mA)	
	1 * Flash	2 * Flash
Normal	65.08	64.87
Stand-By	0.223	0.245
Sleep	0.223	0.253
Read	108.87	159.55
Write	153.43	159.55

The above values are for reference only, it may change according to the flash memory used.

F. Electrical Specifications

Absolute Maximum Rating

Item	Symbol	Parameter	MIN	MAX	Unit
1	$V_{DD}-V_{SS}$	DC Power Supply	-0.3	+5.5	V
2	V_{IN}	Input Voltage	$V_{SS}-0.3$	$V_{DD}+0.3$	V
3	T_a	Operating Temperature (Commercial)	0	+70	°C
4	T_a	Operating Temperature (Industrial)	-40	+85	°C
5	T_{st}	Storage Temperature (Commercial)	-40	+85	°C
6	T_{st}	Storage Temperature (Industrial)	-50	+125	°C

Parameter	Symbol	Min	Typ	MAX	Unit
Operating Temperature (Commercial)	T_a	0	+25	+70	°C
Operating Temperature (Industrial)	T_a	-40	+25	+85	°C
V_{DD} Voltage	V_{DD}	3.0	3.3	3.6	V
		4.5	5.0	5.5	V

G. DC Characters

DC characteristics of 3.3V I/O Cells

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
V _{CK}	Core Power Supply	Core Area	1.62	1.8	1.98	V
V _{CC3IO}	Power Supply	3.3V I/O	3.0	3.3	3.6	V
Temp	Junction Temperature		0	25	115	°C
V _t	Switching threshold	LVTTL		1.5		V
V _{t-}	Schmitt Trigger Negative Going threshold voltage	LVTTL	0.8	1.1		V
V _{t+}	Schmitt Trigger Positive Going threshold voltage			1.6	2.0	V
V _{ol}	Output Low voltage	I _{ol} = 2 ~ 16 mA			0.4	V
V _{oh}	Output High voltage	I _{oh} = 2 ~ 16 mA	V _{CC3IO} - 0.4			V
R _{pu}	Input Pull-Up Resistance	PU=high, PD=low	40	75	190	KΩ
R _{pd}	Input Pull-Down Resistance	PU=high, PD=low	40	75	190	KΩ
I _{in}	Input Leakage Current	V _{in} = V _{CC3I} or 0			10	μA
I _{oz}	Tri-state Output Leakage Current		-10	±1	10	μA

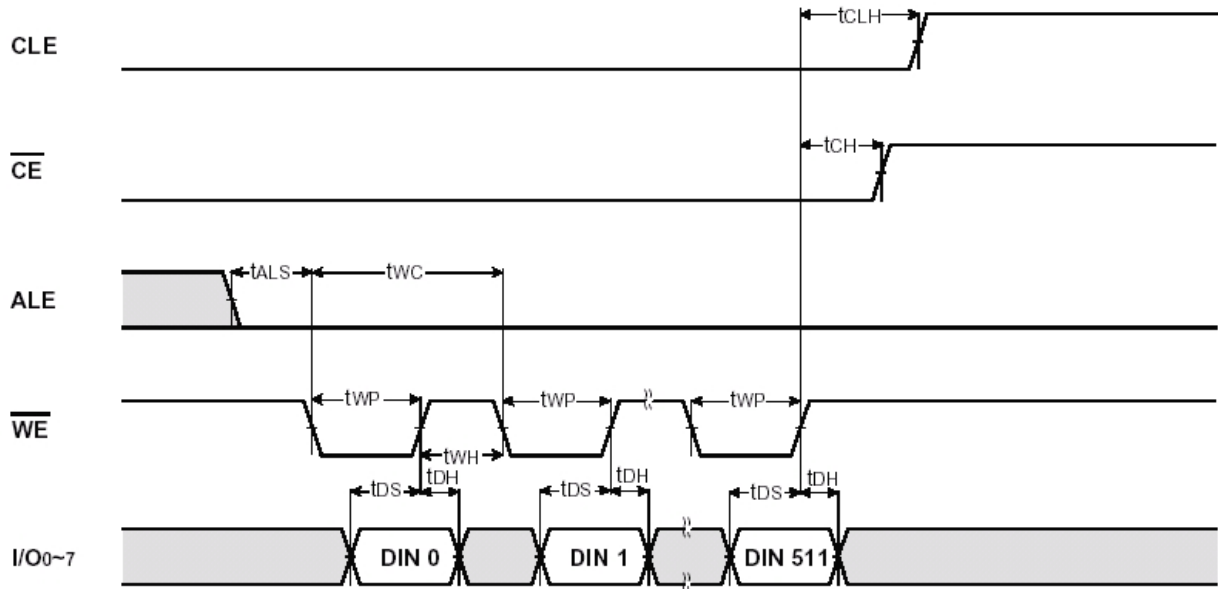
H. AC Characters

H1. Flash Memory Interface Timing

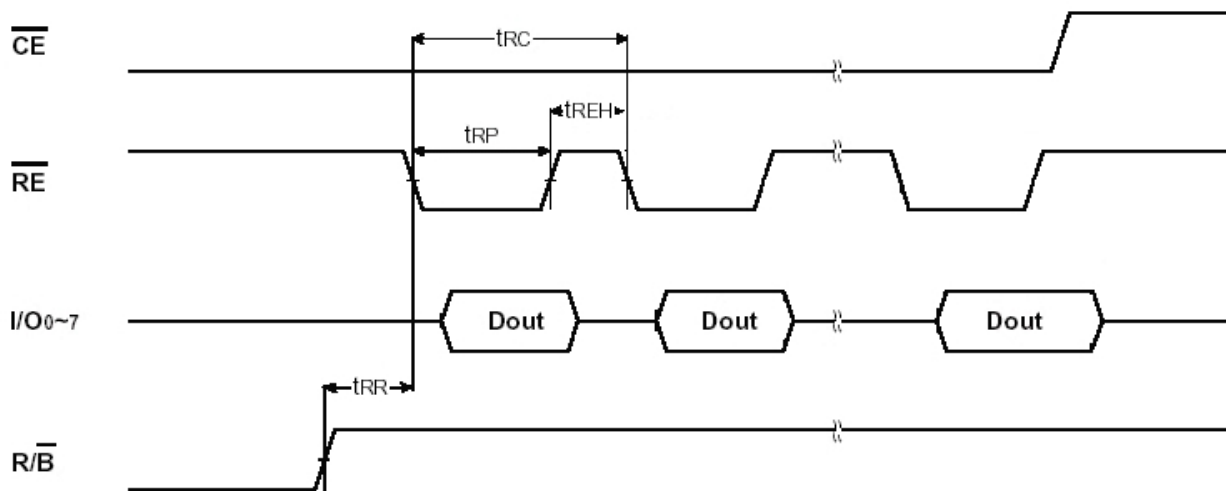
NAND Flash Memory Interface Timing

Parameter	Symbol	Min	Max	Unit
CLE Set-up Time	t _{CLS}	0	-	ns
CLE Hold Time	t _{CLH}	10	-	ns
CE Setup Time	t _{CS}	0	-	ns
CE Hold Time	t _{CH}	10	-	ns
WE Pulse Width	t _{WP}	25	-	ns
ALE Setup Time	t _{ALS}	0	-	ns
ALE Hold Time	t _{ALH}	10	-	ns
Data Setup Time	t _{DS}	20	-	ns
Data Hold Time	t _{DH}	10	-	ns
Write Cycle Time	t _{WC}	45	-	ns
WE High Hold Time	t _{WH}	15	-	ns
Read Cycle Time	t _{RC}	50	-	ns
/RE Pulse Width	t _{RP}	25	-	ns
/RE High Hold Time	t _{REH}	15	-	ns
Ready to /RE Low	t _{RR}	60	-	ns

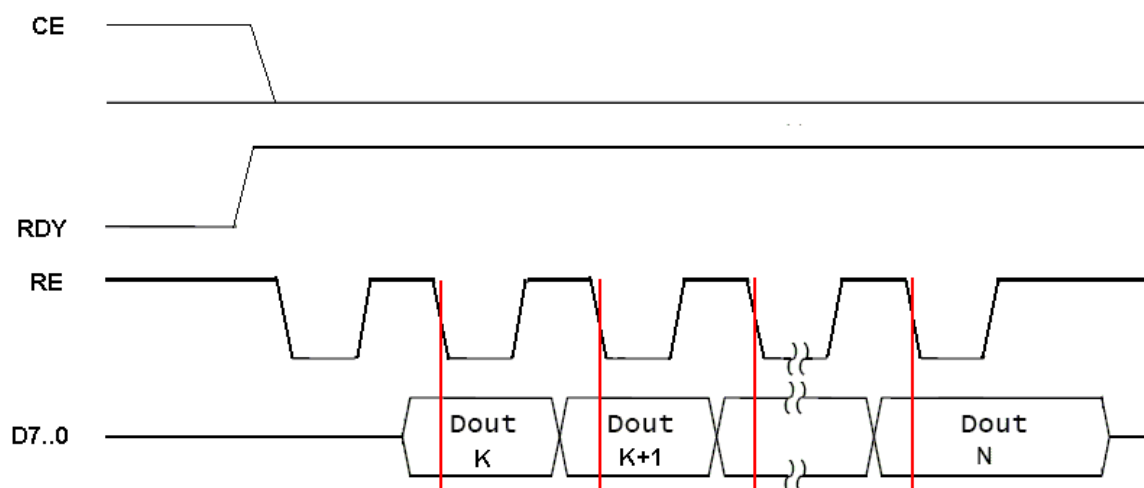
H1.3 Input Data Latch Cycle



H1.4 Sequential Out Cycle after Read (CLE=L, \overline{WE} =H, ALE=L)



H1.5 EDO mode for data latch



EDO mode to latch the data at the negative edge of RE.

I. Package Information

11. 48 Pins

SYMBOL	DIMENSION (MM)			DIMENSION (MIL)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A			1.60			63
A1	0.05		0.15	2		6
A2	1.35	1.40	1.45	53	55	57
b	0.17	0.22	0.27	7	9	11
b1	0.17	0.20	0.23	7	8	12
c	0.09		0.20	4		8
c1	0.09		0.16	4		6
D		9.00 BSC			354 BSC	
D1		7.00 BSC			276 BSC	
E		9.00 BSC			354 BSC	
E1		7.00 BSC			276 BSC	
\bar{e}		0.50 BSC			20 BSC	
L	0.45	0.60	0.75	18	24	30
L1		1.00 REF			39 REF	
R1	0.08			3		
R2	0.08		0.20	3		8
Y			0.075			3
θ	0°	3.5°	7°	0°	3.5°	7°
$\theta 1$	0°			0°		
$\theta 2$	11°	12°	13°	11°	12°	13°
$\theta 3$	11°	12°	13°	11°	12°	13°

NOTE:

1. REFER TO JEDEC MS-026/BBC

2. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION.

3. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE D1 AND E1 ARE

MAXIMUM PLASTIC BODY SIZE DIMENSION INCLUDING MOLD MISMATCH.

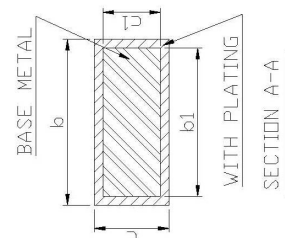
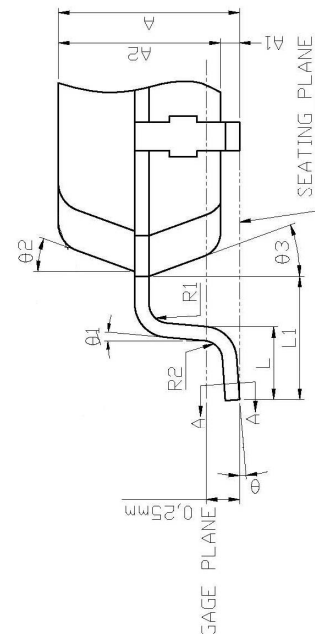
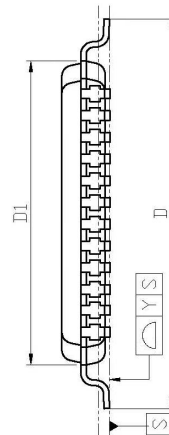
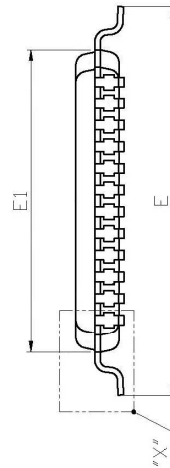
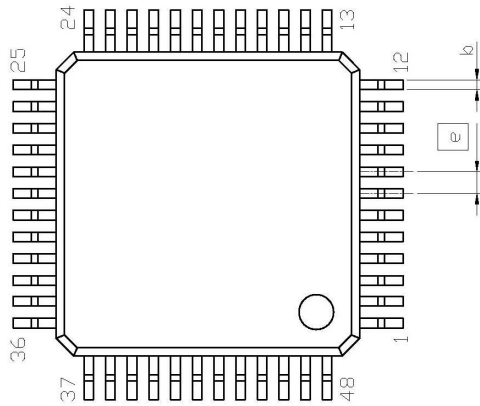
4. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE

DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED

THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm.

5. ALL DIMENSIONS IN MILLIMETERS.

6. Remark-Modify PKG. CODE



TITLE LQFP48 (7x7mm)
PACKAGE OUTLINE
Footprint 2.0mm

SCALE 10 : 1

SHEET 1 OF 1

Detail "X"

SECTION A-A

PROJ.

PROJ.